Reference

COMPUTE PROCESSING MODULE

ATCA-4616
ATCA-4618
ATCA-4648

March 2012 **007-03446-0000**

Revision history

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Preface

About this manual

This manual describes the ATCA-46xx, a compute processing module (CPM), which is fully compliant with AdvancedTCA® (ATCA®). The CPM is designed to be incorporated into High Availability (HA) systems such as the Radisys platforms SYS-6006 and SYS-6010.

Use this manual as a hardware reference for the operation and maintenance of the ATCA-46xx CPM. The manual also provides information on the electrical, the mechanical, and the environmental aspects of the ATCA-46xx CPM. The material presented here is not introductory; it is assumed that you are already familiar with the intended use of the ATCA-46xx CPM in your organization's ATCA platform.

The simplified names "CPM" and "module" will be used in place of "ATCA-46xx CPM" for the body text in the remainder of this manual.

Note: The software material since software release 3.2.0 now resides in the *Software Guide for Management Processors and General Computing Processors* and the *Command Line Interface Reference*. These manuals consolidate the software information for the ATCA modules.

Where to get more product information

Visit the Radisys web site at www.radisys.com for product information and other resources. Downloads (manuals, release notes, software, etc.) are available at www.radisys.com/downloads.

See the following resources for information on the CPM not described in this manual:

- **Installation and initial setup instructions.** The *ATCA-4xxx Compute Processing Module Installation Guide* provides the steps for installing the CPM into a shelf and completing the initial configuration.
- **Platform hardware information.** The CPM is incorporated into platform systems such as the Radisys platforms SYS-6002,SYS-6014, and SYS-6016. For information about the platforms and their shelf hardware, see the appropriate *Platform Hardware Installation Guide* and the Platform Hardware Reference. Each *Installation Guide* provides the steps for installing and setting up the platform's shelf and each *Reference* describes the platform's features and operation.
- **Command line interface (CLI) reference information**. The *Command Line Interface Reference* describes the master CLI and its command modes and serves as a reference for command syntax and options. When referenced in this manual, the simplified name of *CLI Reference* will be used.

- **Software reference information.** The *Software Guide for Management Processors and General Computing Processors* describes software concepts and serves as a reference for procedural and usage information. When referenced in this manual, the simplified name of *Software Guide* will be used.
- **Shelf Manager information.** The *Shelf Management Software Reference* describes the architecture and the operation of the Shelf Manager. The Shelf Manager typically runs on the SCM and controls and monitors operations on the shelf.
- **Update information.** Firmware and software updates may be available for the CPM components from time to time. For information on updating components on the CPM and other modules, see the *Firmware and Software Update Instructions*.

About related Radisys products

The ATCA-46xx CPM is part of the following Radisys platforms: SYS-6002 and SYS-6014/6016. For information on the ATCA product family and other Radisys products, see the Radisys Web site at www.radisys.com.

Standards information

For information about the PCI Industrial Computer Manufacturers Group (PICMG®) and the AdvancedTCA standard, consult the PICMG Web site http://www.picmg.org).

Related documents

Advanced Switching Core Architecture Specification Revision 1.0, Advanced Switching Interconnect Special Interest Group, December 2003.

IEC 60950-1:2005 (Second Edition), International Electrotechnical Commission (www.iec.ch)

Additionally evaluated to *EN 60950-1:2006/A11:2009; National*. Differences specified in the CB Test Report.

Information Technology - Serial Attached SCSI - 1.1 (SAS-1.1), ANSI/INCITS 417-2006

UL 60950-1:2007, 2nd Edition, (*Information Technology Equipment - Safety - Part 1: General Requirements*)

CSA C22.2 No. 60950:2007, 2nd Edition, (*Information Technology Equipment - Safety - Part 1: General Requirements*)

DDR3 SDRAM VLP RDIMM MT36JBZS51272PY – 4GB, Micron.

GR-*1244-CORE Clocks for the Synchronized Network: Common Generic Criteria*, Issue 2, Telcordia, December 2000.

The I^2C Bus Specification Version 2.1, Philips Semiconductor, January 2000.

IEEE Std 1149.1-2001 Test Access Port and Boundary-Scan Architecture, IEEE Computer Society, June 23, 2001.

IEEE Std 802.3-2002 Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications, IEEE Computer Society, March 8, 2002.

Intelligent Platform Management Interface Specification v1.5, Revision 2.0, Intel Corporation; Hewlett Packard Company, NEC Corporation, and Dell Computer Corporation.

Linux PAM Modules web site. http://www.kernel.org/pub/linux/libs/pam/modules.html

MSP20B01B Backplane External Product Specification Revision 1.0, Intel, August 31, 2001.

PICMG 3.0 Advanced Telecommunications Computing Architecture R3.0, PCI Industrial Computer Manufacturers Group, March 24, 2008

PICMG 3.1 R1.0 Specification, Ethernet/Fibre Channel for AdvancedTCA Systems, PICMG, January 22, 2003

PICMG AMC.0 R2.0 Advanced Mezzanine Card Base Specification, PCI Industrial Computer Manufacturers Group, November 15, 2006

PM8380 QuadSMX 3G Quad SATA/SAS Mux/Demux for 3G, PMC-2031101, Issue 8, PMC-Sierra, April 2005

Serial ATA Revision 2.5, Serial ATA International Organization, October 27, 2005

Platform Management FRU Information Storage Definition v1.0, Revision 1.13.

Integrated RAID for SAS User's Guide, http://www.lsi.com/DistributionSystem/AssetDocument/files/docs/techdocs/storage_stand_prod/sas/ir_sas_ug.pdf from LSI Logic Corporation.

Electrostatic discharge

WARNING! This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operating life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep each carrier in its ESD shielding bag until you are ready to install it.
- Before touching a carrier, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the carrier only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold carrier only by its edge and mounting hardware. Avoid touching PCB components and connector pins.

For further information on ESD, visit www.esda.org.

Notational conventions

This manual uses the following conventions

BoldText	A keyword.
ItalicText	File, function, and utility names.
`MonoText`	Screen text and syntax strings.
`BoldMonoText`	A command to enter.
`ItalicMonoText`	Variable parameters.
Brackets [ ]	Command options.
Curly braces { }	A grouped list of parameters.
Vertical line |	An “OR” in the syntax. Indicates a choice of parameters.

All numbers are decimal unless otherwise stated.

Chapter 1

Product Overview

Introduction

The ATCA-46xx Compute Processing Module (CPM) is a high-end, general-purpose computing module that provides multi-core processing power and multiple data-storage options within a single Advanced Telecommunications Computing Architecture (ATCA) slot.

The remaining sections in this chapter present the major features, specifications compliance, and product options that apply to the ATCA-46xx CPM.

Major features

The following major features apply to the ATCA-46xx CPM:

- Dual Intel® Xeon® E5-2400 family 64-bit multi-core processors using 32-nm process technology
- Intel C600 series Platform Controller Hub (PCH)
- Multiple GbE interfaces
- Fabric interface supporting 40 GbE connections
- Intelligent Platform Management Controller (IPMC)
- CPU Complex FPGA (CC FPGA)
- Redundant 64 Mb SPI Boot Flash devices
- eUSB Flash Memory modules (optional)
- Trusted Platform Module (TPM)
- MXM graphics module (optional)
- Onboard SATA SSD drives (optional)

Supported external interfaces

The ATCA-46xx CPM supports both internal and external interfaces. Internal interfaces include the buses and communication protocols that are fully contained within the CPM blade or are included within the front panel, backplane, or RTM external interfaces. The following external interfaces are supported for the ATCA-46xx CPM:

- Front panel interfaces:
  - Dual USB connectors (Type A)
  - RJ-45 serial port connector (RS-232, COM1)
  - Dual RJ-45 GbE connectors
  - Mini DisplayPort connector (when optional MXM video module is installed)
  - Reset push button
  - Hot Swap extraction switch (part of ejector handle)
  - LED indicators
    - Blue hot swap LED
    - Red or amber out of service (OOS) LED
    - Green/amber user-defined (APP) LED
    - Green HDD activity LED
    - Green/amber Link/Speed/Activity LEDs (each Base/Fabric interface)
- Backplane interfaces (ATCA Zone 2 connectors)
- RTM interface (ATCA Zone 3 connectors)

Specification compliance

The ATCA-46xx CPM complies with the following specifications:

- PCI Industrial Computers Manufacturers Group (PICMG) 3.0 R2.0 ECN0002 Advanced Telecommunications Computing Architecture (ATCA) specification
- PICMG 3.1 R2.0 Ethernet over ATCA (Options 1 and 9) specification
- European requirements for hazardous materials (ROHS 6/6)
- Mechanical and environmental specifications:
  - CE
  - FCC Class A
  - VCCI-A
  - cUL
  - NEBS Level 3 (designed to meet)
- Safety specifications:
  - USA - UL 60950-1
  - Canada - CSA 22.2 #60950-1
  - EU - EN 60950-1
  - Other - IEC 60950-1
- Electromagnetic Compatibility (EMC) specifications:
  - Emissions; radiated/conducted (FCC Part 15 and EN 55022:2006)
  - Immunity; ESD (EN 61000-4-2), radiated (EN 61000-4-3), fast transient/burst (EN 61000-4-4), surge voltages (EN 61000-4-5), conducted (EN 61000-4-6), magnetic field (EN 61000-4-8)

Product options

The ATCA-46xx CPM has the following product options:

- A4616-CPU-Base - The basic low-power CPM with 10G Fabric interface, dual Intel Xeon six core processors, and no installed memory.
- A4618-CPU-Base - The basic high-power CPM with 10G Fabric interface, dual Intel Xeon eight core processors, and no installed memory.
- A4648-CPU-Base - The basic high-power CPM with 40G Fabric interface, dual Intel Xeon eight core processors and no installed memory.
- A4600-MEM-xxGB - A memory kit consisting of twelve yGB DDR3 VLP registered DIMM (RDIMM) modules that provides a total of xxGB of RDIMM memory for the CPM.
- A4600-eUSB-32GB - A memory expansion option with two eUSB NAND Flash modules with a capacity of 16GB per module.
- A4600-DSSDMXM-M - A mass storage option with two 1.8“ Solid State Disk (MLC SSD) modules of 64GB capacity each. The SSD modules mount on a dual drive carrier that connects through the MXM connector to the onboard SATA ports of the CPM.

For a current listing of product options, visit the ATCA-46xx product page at www.radisys.com.

Chapter 2

Hardware Description

Introduction

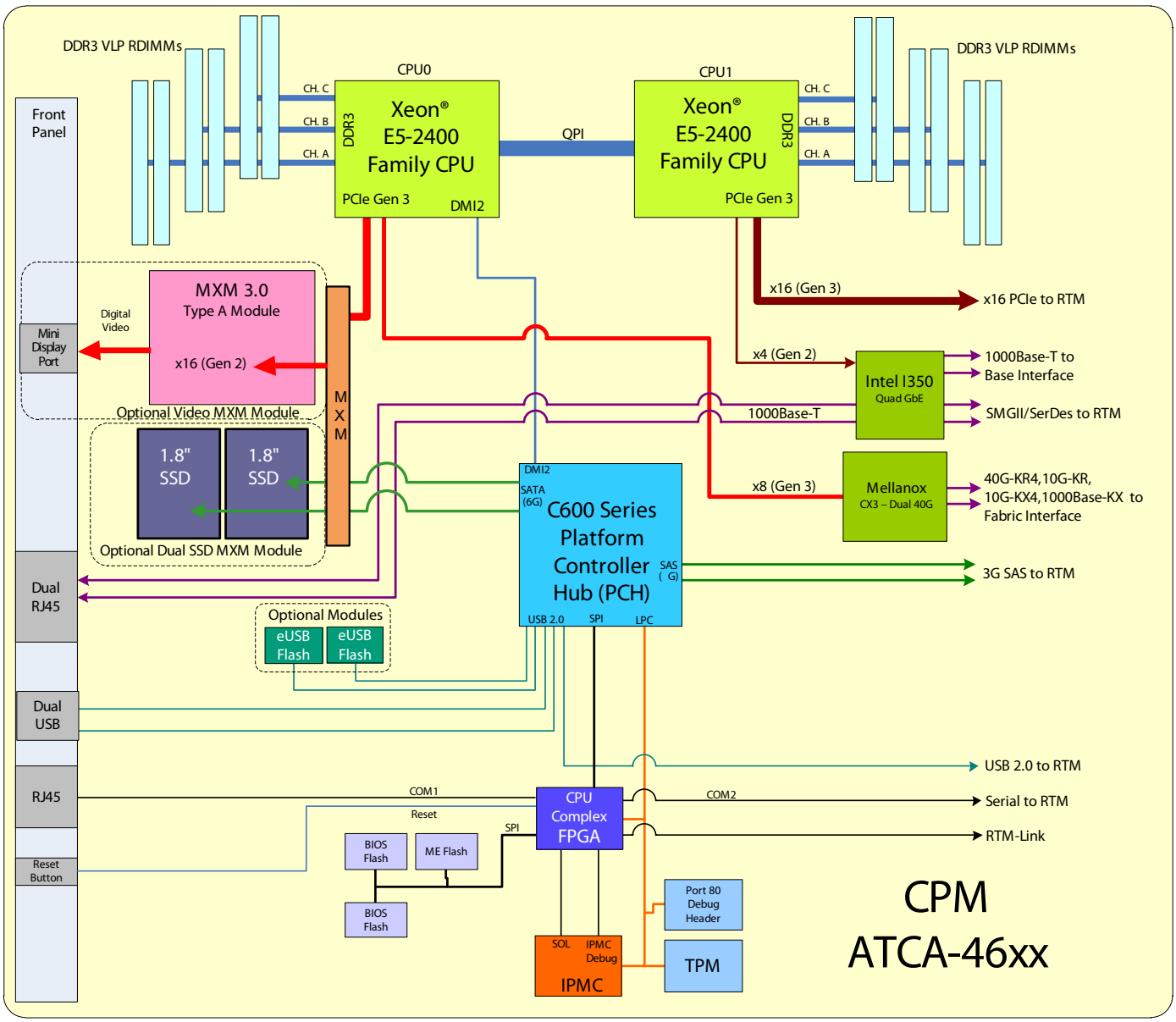
The ATCA-46xx Compute Processing Module (CPM) uses a number of hardware components to implement the functions required of an ATCA node. The major hardware components in the ATCA-46xx CPM are as follow:

- Dual E5-2400 family processors mounted in FCLGA1356 sockets
- Intel C600 series Platform Controller Hub (PCH) chip that supports the major I/O functionality on the CPM.
- Sockets for six registered DIMM (RDIMM) or Load Reduced DIMM (LRDIMM) memory modules per processor or twelve modules total. Supported RDIMMs and LRDIMMs include 800, 1066, or 1333 MHz DDR3 modules of 1, 2, 4, 8, or 16 GB capacity for a total of up to 96 GB per processor or 192 GB total for the module.
- Intel I350 quad Gigabit Ethernet controller that supports two GbE Ethernet ports connected to the Base Interface channels and GbE Ethernet ports routed to the CPM front panel or the RTM interface.
- A Mellanox dual 40 GbE controller that provides two 40 Gb Ethernet ports for the CPM fabric interface.
- Heat sinks to dissipate heat generated by the E5-2400 family processors, the PCH, and the 40 GbE controller.
- Front panel connectors for serial, video, USB, and Ethernet.
- Front panel LEDs that indicate CPM condition and status information.
- Zone 1 (P10), Zone 2 (J20 and J23), and Zone 3 (J30 and J31) connectors to the backplane and RTM.
- (Optional) MXM 3.0 type A video module
- (Optional) One or two 1.8” microSATA SSD drives mounted in an MXM DSSD module tray
- (Optional) One or two eUSB Flash modules

Functional block diagram

Figure 1 is a functional block diagram that indicates major hardware components of the CPM.

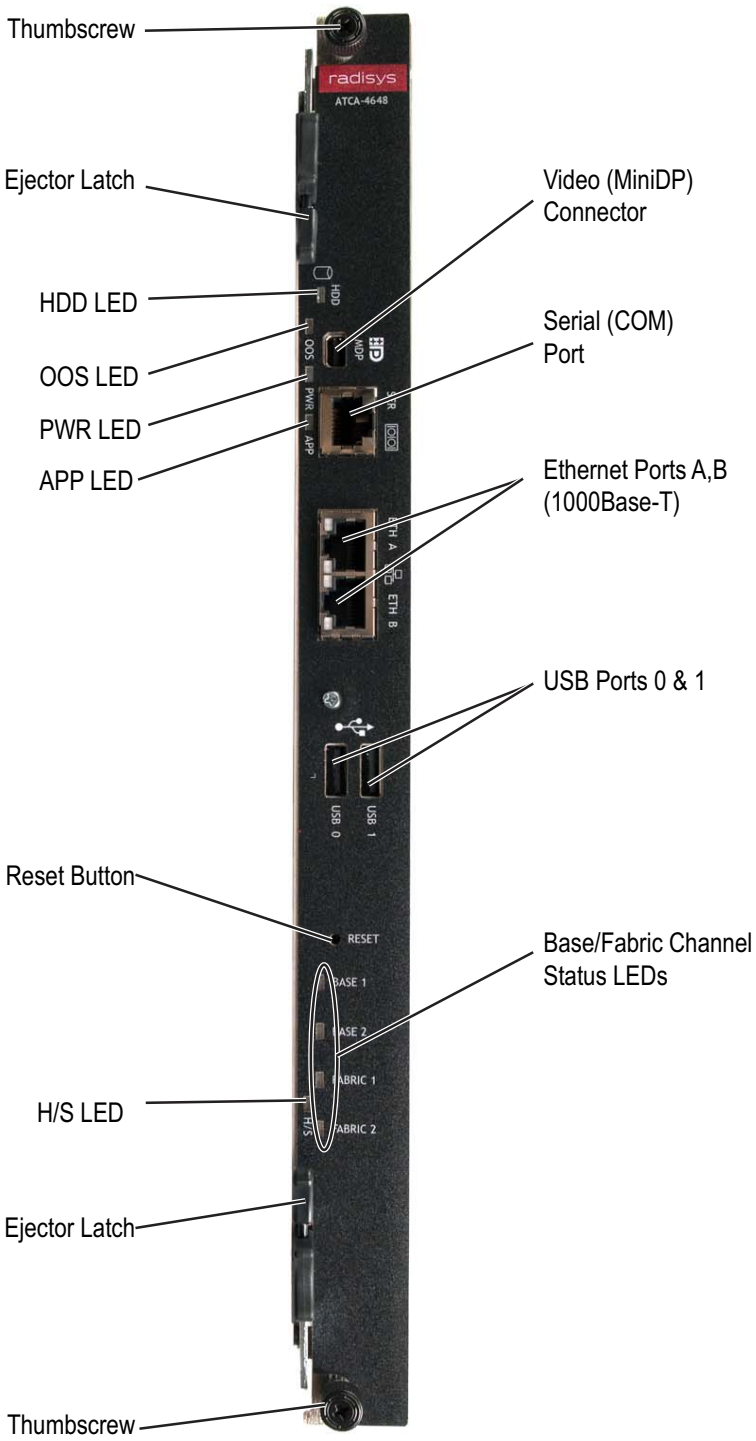
Figure 1. ATCA-46xx Functional Block Diagram



ATCA-46xx front panel components

The following sections use text, figures, and lists to identify the physical features of the CPM. Figure 2 shows the CPM front panel and calls out the major features.

Figure 2. Front Panel Components



Front panel connectors

There are connectors for four separate interfaces on the front panel. Plugging into the connectors is straightforward, but the underlying interfaces need some explanation.

The serial (COM) RJ45 connector is an RS232 serial interface with the pinout listed in Table 39 on page 108.

The USB0 and USB1 connectors support USB 2.0 transactions. A USB cable connected to a single device up to 5 meters away can be used with the front panel USB connectors. Transfers at up to 480 Mbps and continuous load currents up to 500 mA are supported with these USB ports. Refer to Table 40 on page 108 for the USB connector pinout.

The miniDisplayPort connector can be connected to a digital monitor if the MXM port has a video module installed. Refer to the video module documentation for operation details for this option. Refer to Table 42 on page 109 for the connector figure and pinout listing of the miniDisplayPort connector. During normal operation there is no need to attach a monitor to this connector.

The two front panel Ethernet connectors provide interfaces to GbE ports with a peak available bandwidth of 100Mbps or 1Gbps. Figure 3 shows one of the front panel Ethernet connectors and calls out the Port Status and Link Status LEDs that are part of the connector.

Figure 3. Front Panel Ethernet Connectors

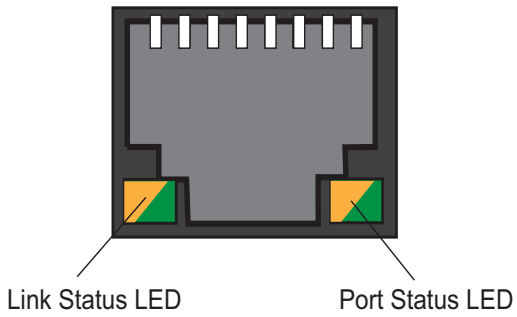


Table 1 lists the meanings assigned to the light color/activity of each LED on the Ethernet connector.

Table 1. Front Panel Ethernet Connector LEDs

LED Designation	Indication	Meaning
Port Status LED	Steady Green	Port enabled
	Steady Amber	Port in standby mode
	No light	Port disabled
Link Status LED	Steady Green	Linked at 1 Gbps peak bandwidth
	Blinking Green	Activity at 1 Gbps peak bandwidth
	Steady Amber	Linked at 10/100 Mbps peak bandwidth
	Blinking Amber	Activity at 10/100 Mbps peak bandwidth
	LED off	No link

Front panel LEDs

The front panel LEDs can be separated into two major groups; the edge LEDs along the left (bottom) edge of the front panel and the Base/Fabric channel status LEDs.

Table 2 describes the status and activity LEDs along the left (bottom) edge of the front panel.

Table 2. Front Panel Edge Activity/Status LEDs

LED Designation	Indication	Meaning
HDD (Hard Disk Drive) LED	Short Green blink	HDD being accessed
	LED off	No HDD activity, or not installed
OOS (Out-of-Service) LED	Steady Amber LED	LED color and On/Off state controlled by the IPMC and user-defined application.
	Steady Red LED	
	LED off	Normal operation
PWR (Health) LED	Steady Green LED	Power ON, health good
	Steady Amber LED	Power ON, health not good
	LED off	Power OFF
APP (Customer-defined application) LED	Steady Green LED	Controlled by the IPMC, with functionality defined by the system implementer[a]
	Steady Amber LED	
	LED off	
H/S (Hot Swap Status) LED[b]	Short Blue blink	M5, FRU deactivation request or M6, FRU deactivation in process
	Steady Blue LED	M1, FRU inactive; ready for hot swap
	Long Blue blink	M2, FRU activation request
	LED off	M0, FRU not installed, or M3, FRU activation in process, or M4, FRU active

[a] The user application can control LED color and illumination using the Set FRU LED State IPMI command. LED illumination can be turned on or off, the LED can be configured to blink, or the lamp test function can be enabled. To use the command, specify the FRU ID, LED ID (which is "1" for the OOS LED), LED function, LED on duration, and illumination color. Command usage is described in the PICMG specification, FRU LED Control commands, section 3.2.5.6.

[b] LED state and blink frequency controlled by the IPMC.

The IPMC uses GPIO pins to control the hot swap and power LEDs. The IPMC supplies default states for the LEDs and responds to sensor readings, GPIO inputs, and IPMI commands from other entities to change LED states.

Table 3 lists the meanings assigned to the light color/activity of each Base/Fabric LED.

Table 3. Base/Fabric Channel LEDs

Channel	Indication	Meaning
Base Channel 1 or Base Channel 2	Steady Green	Linked at 1 Gbps peak bandwidth
	Blinking Green	Activity at 1 Gbps peak bandwidth
	Steady Amber	Linked at 10/100 Mbps peak bandwidth
	Blinking Amber	Activity at 10/100 Mbps peak bandwidth
	LEDs off	Channel not configured or not in use
Fabric Channel 1 or Fabric Channel 2	Steady Green	Linked at 10/40 Gbps peak bandwidth
	Blinking Green	Activity at 10/40 Gbps peak bandwidth
	Steady Amber	Linked at 1/10 Gbps peak bandwidth
	Blinking Amber	Activity at 1/10 Gbps peak bandwidth
	LEDs off	Channel not configured or not in use

Note: The Fabric channel LEDs can be either green or amber when linked or indicating activity at 10 Gbps. This is because in one configuration 10 Gbps is the low range output from the controller while in another configuration it is the high range output. The LED indicates the low/high range output, not the actual link speed.

Reset and hot swap switches

The CPM front panel Reset button (switch) is recessed and can normally be pressed only with a thin, pointed object such as a pencil or stylus. A callout in Figure 2 points out the Reset button on the CPM front panel. The Reset button performs a platform reset of the CPM. A platform reset returns all registers and devices (except the IPMC) to their default state.

The ejector latches and thumbscrews are considered hot swap hardware components. Both thumbscrews must be unscrewed in order to remove the CPM from its slot. The bottom lock and ejector switch must be disengaged in order to signal to the IPMC that a CPM hot swap is desired. The IPMC then controls the hot swap LED and monitors the process.

Headers and jumpers

Refer to *Appendix C, Onboard switches, headers, and connectors,* on page 114 for tables detailing the header and jumper callouts.

Rear panel connectors

The CPM supports E-Key control by describing its backplane interfaces to the Shelf Manager.

Alignment keys

The CPM implements the K1 and K2 alignment blocks at the top of Zone 2 and Zone 3, as required by the PICMG 3.0 specification. The Zone 2 alignment block (K1) is assigned a keying value of 11. The Zone 3 alignment block (K2) is set to allow insertion of ATCA-46xx-compatible RTMs.

Zone 1 connector

The connectors in Zone 1 provide redundant -48VDC power and Shelf Management signals to the boards. The power control interface to the IPMC is through the backplane connector P10 (Zone 1 power distribution connector). Refer to Table 44 on page 111 for details.

Zone 2 connectors

The connectors in Zone 2 provide the connections to the Base Interface and Fabric Interface. All Fabric connections use point-to-point 100 Ω differential signals. Zone 2 is called "Fabric Agnostic" which means that any Fabric that can use 100 Ω differential signals can be used with an AdvancedTCA backplane.

Backplane connector J20 provides Zone 2 connections to the synchronization clocks and to the AMC update channels. For detailed information about the connector itself, refer to Table 45 on page 112.

Backplane connector J23 is the ATCA data transport connector, which provides Zone 2 connections for two 10/100/1000BASE-T Ethernet Base channels and two 10GBASE-BX4 Ethernet Fabric channels. For more information about the J23 backplane connector, refer to Table 46 on page 112.

Zone 3 connectors

The CPM includes the standard Zone 3 backplane interface to provide connectivity to an optional RTM, such as the ATCA-5400. This interface consists of two connectors: J30 for common and maintenance signals, and J31 for SerDes (serialization/deserialization connectivity). For details, refer to Table 47 on page 113 and Table 48 on page 113.

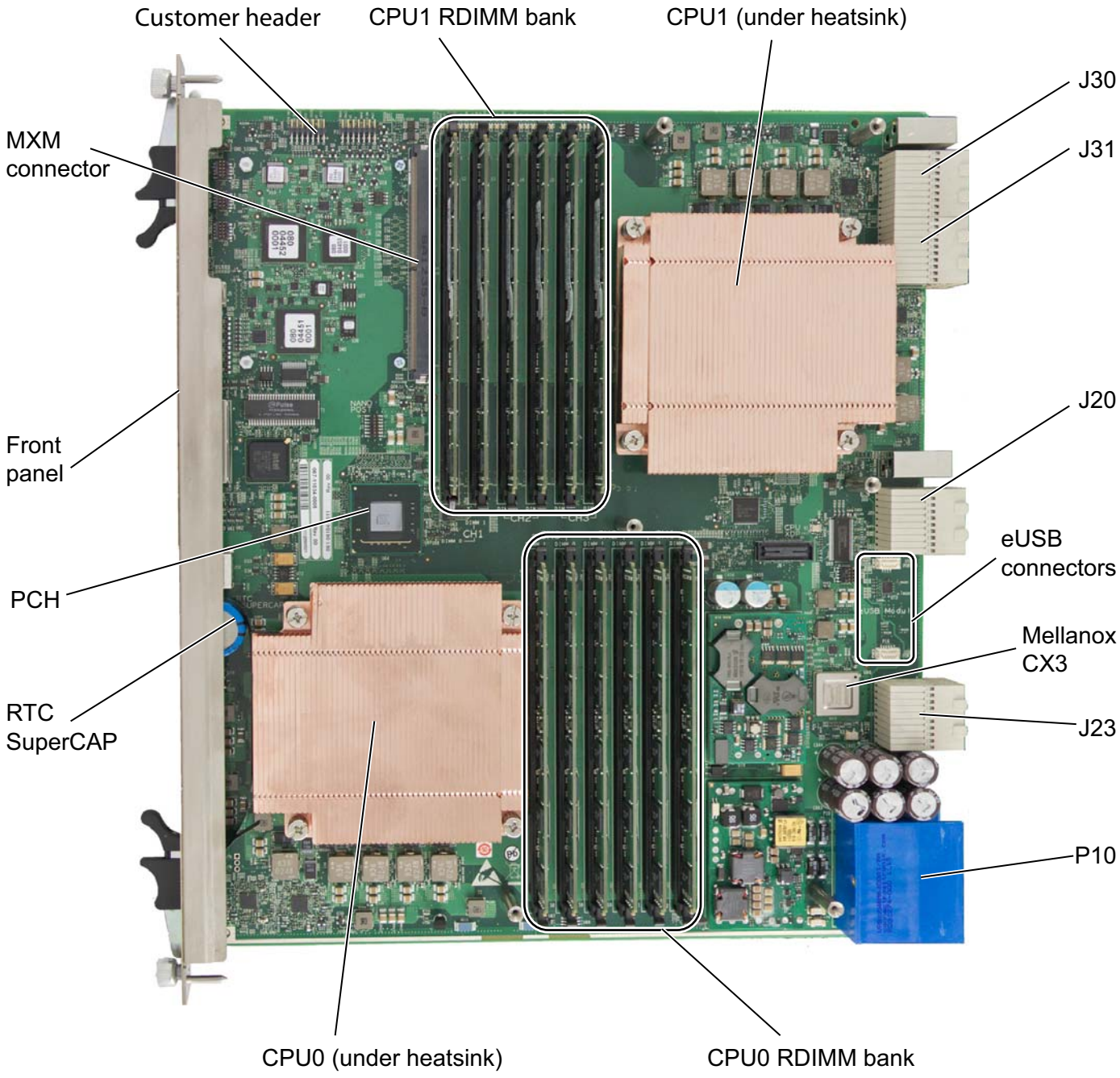
The electrical connections between the CPM and the associated RTM include:

- Switched +3.3V and +12V power, under the control of the IPMC
- One configurable PCI Express port
- One USB 2.0 Port
- IPMB-L I^2C Bus for an MMC on an RTM
- IPMC Hot Swap control signals
- RTM-Link interface to CPU Complex FPGA
- Serial Port (3.3V signals)
- Two 1Gbps SerDes/SGMII ports
- Two SFP I^2C ports for SGMII support
- System reset signal
- JTAG interface
- PCH SMBus connection

ATCA-46xx board components

During normal operation the CPM board components are covered by the CPM cooling shroud sheet metal (side panel). This sheet metal must be removed to see and gain access to removable board components, jumper blocks, or headers. Figure 4 shows the CPM board layout and calls out the major components and other features.

Figure 4. CPM Board Layout



Heatsinks

The CPU heatsinks are called out in Figure 4. In addition to the CPU heatsinks, the Intel C600 series PCH, and the Mellanox CX3 10/40 GbE controller each have individual heatsinks. The CPM incorporates a large heatsink covering each processor plus the additional heatsinks for other onboard high power devices to support a maximum CPM subsystem power dissipation of up to 50W. In addition, the installed RDIMM modules might also have their own heatsinks or other thermal solution.

WARNING! All heatsinks on the CPM are critical for proper board operation. Make sure all heatsinks have adequate mechanical and thermal contact with their associated components and ensure the sheet metal cooling shroud is secured in place before installing the CPM in its slot.

Major components

Figure 4 calls out the following major components on the CPM board:

- Two Intel Xeon E5-2400 family processors. Refer to *Intel® Xeon® E5-2400 family processor* on page 25 for detailed information.
- Sockets for twelve registered DIMM memory modules (six for each CPU). Refer to *DIMM memory* on page 28 for detailed information.
- The C600 series PCH component. Refer to *Intel C600 series Platform Controller Hub (PCH)* on page 29 for detailed information.
- Mellanox CX3 dual 10/40 GbE Ethernet controller. Refer to *Mellanox dual 40GbE controller* on page 36.

In addition to the components called out in Figure 4, the following components (indicated in the Figure 1 block diagram) control significant portions of CPM operation:

- The H8S/2400 series IPMI controller. Refer to *IPMI controller* on page 33 for more detailed information.
- CPU Complex FPGA (*CPU Complex (CC) FPGA* on page 34) and IPMC FPGA (*IPMI controller* on page 33) modules.
- The Intel I350 quad GbE Ethernet controller. Refer to *Intel I350 quad GbE Ethernet controller* on page 36.
- Clock synthesizer subsystem. Refer to *Clock synthesizer subsystem* on page 37.
- Reset subsystems. Refer to *Reset subsystems* on page 37.
- Trusted Platform Module (TPM). Refer to *Trusted Platform Module (TPM)* on page 42.
- Optional MXM Type A video module. Refer to *MXM type A video module (optional)* on page 43.
- Optional 1.8” Solid State Drive (SSD) module(s). Refer to *1.8” Solid State Drive (SSD) module (optional)* on page 43.
- Optional eUSB Embedded Flash module(s). Refer to *eUSB Embedded Flash module (optional)* on page 44.

Intel® Xeon® E5-2400 family processor

The CPM uses two Intel® Xeon E5-2400 family multi-core, 64-bit processors built using a 32-nm process. The E5-2400 processor includes a 3-channel memory controller, QuickPath interconnect, and integrated I/O for PCI Express support. The processor cores share an up to 20MB cache and include support for the Execute Disable Bit, Speed-Step, Virtualization, Streaming SIMD Extensions, Hyper-Threading, Turbo Boost, and TXT. The ATCA-46xx CPM E5-2400 processors have a maximum thermal power dissipation (TPD) ranging from 50 W to 70 W depending on configuration.

Table 4 and Table 5 provide the major processor specifications.

Table 4. CPU bus specifications

Processor	Number of Cores	Number of Threads	QPI Speed	DDR3 Speed	Last Level Cache Size
LV70W-8C	8	16	8.0 GT/s	1333 MHz	20 MB
LV60W-6C	6	12	7.2 GT/s	1333 MHz	15 MB
LV50W-4C	4	8	6.4 GT/s	1333 MHz	10 MB

Table 5. CPU thermal specifications

Processor	Thermal Design Power (TDP)	Case temperature (long term operating)	Case temperature (short term* operating)
LV70W-8C	70W	78.1°C	93.2°C
LV60W-6C	60W	73.4°C	88.4°C
LV50W-4C	50W	77.4°C	92.4°C
* ***Note***: Short term operating = 360 hours per year (or less)			

Adaptive thermal monitor for processor protection

The CPU case temperature must remain within the specified operating range in order to maintain reliability over the life of the processor. The CPU includes an adaptive thermal monitor (ATM) to help control the processor temperature. The ATM selects between voltage and frequency control and internal clock modulation to reduce processor power and to activate the thermal control circuitry.

Each CPU includes a single digital thermal sensor (DTS) that continuously measures the temperature at the processing cores and provides processor die temperature information that represents the worst case temperature for all cores. The DTS data represents the difference between the current die temperature and the temperature at which the ATM activates the thermal control circuitry. The IPMC accesses DTS information through the PCH Management Engine (ME) over the platform environmental control interface (PECI). The ME independently monitors the DIMM, CPU, and PCH temperatures and relays that information to the IPMC over the I^2C Bus.

Integrated Memory Controller (IMC)

The integrated memory controller incorporated into each E5-2400 family processor supports three channels of DDR3, each channel with 64 data bits and 8 ECC bits. The CPM supports up to six registered VLP RDIMMs per socket (two per channel) for a system total of twelve RDIMMs. Table 6 lists the supported RDIMM memory types of the CPM and provides the required specifications for the modules.

Table 6. Supported Memory Types

Mem Rank x Data Width	Operating Voltage	DIMMs per Channel	Memory per DIMM	Speed (MT/s)
Registered DIMM (RDIMM) with ECC				
Single rank x 8 bits	1.5 v	One or Two	1, 2, 4 GB	1066/1333 MHz
Single rank x 8 bits	LV - 1.35 v	Two	1, 2, 4 GB	1066 MHz
Dual rank x 8 bits	1.5 v	One or Two	2, 4, 8 GB	1066/1333 MHz
Dual rank x 8 bits	LV - 1.35 v	Two	2, 4, 8 GB	1066 MHz
Quad rank x 8 bits	1.5 v or LV - 1.35 v	One or Two	4, 8, 16 GB	800 MHz
Single rank x 4 bits	1.5 v	One or Two	2, 4, 8 GB	1066/1333 MHz
Single rank x 4 bits	LV - 1.35 v	Two	2, 4, 8 GB	1066 MHz
Dual rank x 4 bits	1.5 v	One or Two	4, 8, 16 GB	1066/1333 MHz
Dual rank x 4 bits	LV - 1.35 v	Two	4, 8, 16 GB	1066 MHz
Quad rank x 4 bits	1.5 v or 1.35 v	One or Two	8, 16, 32 GB	800 MHz
Load Reduced DIMM (LRDIMM) with ECC				
Quad rank x 8 bits	LV - 1.35 v	One	8, 16 GB	1066 MHz
Quad rank x 8 bits	LV - 1.35 v	Two	8, 16 GB	800 MHz
Quad rank x 8 bits	1.5 v	One	8, 16 GB	1066/1333 MHz
Quad rank x 8 bits	1.5 v	Two	8, 16 GB	1066 MHz
Quad rank x 4 bits	LV - 1.35 v	One	16, 32 GB	1066 MHz
Quad rank x 4 bits	LV - 1.35 v	Two	16, 32 GB	800 MHz
Quad rank x 4 bits	1.5 v	One	16, 32 GB	1066/1333 MHz
Quad rank x 4 bits	1.5 v	Two	16, 32 GB	1066 MHz

The integrated memory controller supports up to four memory modes, but the CPM uses only the Independent mode (highest performance) in which RDIMMs can be placed in any of the three channels and there are no matching requirements for rank or DIMM speed between channels. A burst-length of 8 is used, and the memory controller is configured to interleave the memory map across the three channels.

The IMC provides the following tools to support memory reliability and peak operation:

- SDDC (Single Device Data Correction) algorithm that can detect and correct any error within a x4 device in independent mode.
- DRAM thermal management either by DRAM throttling or by performing a 2X refresh to the memory channels.

QuickPath Interconnect (QPI)

The Quickpath interconnect (QPI) provides a point-to-point contact between the E5-2400 family processors. The QPI interface is 20 lanes wide under full operation and is the communication path between the CPUs. Data of any width is converted to packets and then sent serially over the QPI link. The E5-2400 supports QPI speeds of 6.4 GT/s to 8.0 GT/s depending on the installed processor.

PCI Express

The integrated I/O module on each E5-2400 family processor provides 24 PCI Express lanes that are capable of Gen1 (2.5 GT/s), Gen2 (5.0 GT/s) and Gen3 (8.0 GT/s) speeds. The lanes are split into a x16 and a x8 port and both can be divided into x8, x4, x2 and x1 ports. CPU0 also uses a Gen 2 Direct Media Interface (DMI) port that can be configured for either DMI for PCH connectivity or used as a Gen2 x4 PCI Express port. Table 7 shows the PCI Express port mapping for each CPU on the CPM.

Table 7. PCI Express Port Mapping

CPU	Port#	Port Width	PCI Express Peripheral
CPU0	PE1(A,B)	x8	Fabric Ethernet Controller
CPU0	PE3(A,B,C,D)	x16	MXM
CPU0	DMI2	x4	Patsburg DMI2 interface
CPU1	PE1A	x4	I350 Base/Front/RTM GbE controller
CPU1	PE1B	x4	Update Channel
CPU1	PE3A*	x4	RTM PCI Express port 0
CPU1	PE3B*	x4	RTM PCI Express port 1
CPU1	PE3CD*	x8	RTM PCI Express port 2
* ***Note***: As with the CPU0 mapping, CPU1 Ports PE3(A,B,C,D) can alternately be combined to form a single x16 interface.			

Memory

The CPM uses memory such as the built-in processor cache, standard RAM, and memory external to any of the existing board components. The CPM supports the following types of memory:

- DIMM memory - Registered Dual In-line Memory Modules (RDIMM) and Load Reduced Dual In-line Memory Modules (LRDIMM)
- Non-volatile on-board memory - Flash memory devices.
- Optional on-board user memory - One or two eUSB Flash modules.
- Mass storage - One or two 1.8” SSD modules and any RTM hard disk drives (HDDs).

The following sections provide more detailed information.

DIMM memory

This memory is directly addressed by the internal memory controller of each E5-2400 family processor. Due to the board height limitations posed by the ATCA PICMG specifications, only Very Low Profile (VLP) Dual In-line Memory Module (DIMM) modules are supported with the CPM. The Registered DIMM (RDIMM) memory used on the CPM is buffered by integral registers and has built-in Error Correcting Code (ECC) bits to support more reliable operation. As part of the installation process for the CPM, up to twelve RDIMM modules (six per processor, from 1GB to 16GB each) must be installed in the CPM DIMM sockets. Refer to *Adding or replacing memory modules* on page 73 for the installation procedures.

Non-volatile on-board memory

The CPM non-volatile memory is mainly comprised of the following elements:

- The two 64-Mbit Flash BIOS boot and redundant boot devices.
- The 64-Mbit ME Flash holding the redundant ME firmware.
- IPMI non-volatile memory stores IPMC private data and board FRU information.
- The optional eUSB NAND Flash memory modules are available for user applications and data.

External memory options

The following external memory options are available for the CPM:

- Embedded NAND Flash modules. One or two eUSB NAND Flash modules.
- 1.8” micro Solid State Disk (SSD) drives. One or two µSATA SSD modules. This option requires the Radisys Dual SSD (DSSD) MXM module for mounting the SSD modules.
- RTM-installed hard disk drives (HDDs). Number and capacity dependent on the RTM.

Intel C600 series Platform Controller Hub (PCH)

The Intel C600 series Platform Controller Hub (PCH) provides a connection point between various I/O components and the E5-2400 family Xeon processors used on the CPM. The PCH provides controllers for the following interfaces:

- Direct Media Interface
- Universal Serial Bus
- Serial Addressed SCSI (SAS)
- Serial ATA (SATA)
- Low Pin Count (LPC) Bridge
- Serial Peripheral Interface (SPI)
- Real-Time Clock (RTC)
- SMBus/I^2C bus
- Management Engine

Refer to Figure 1 to identify the interfaces and the devices controlled by the PCH. The following sections provide details on the interfaces and associated controllers of the PCH.

Direct Media Interface (DMI)

There is a Direct Media Interface Gen 2 (DMI2) 4x link between the PCH and CPU0 that is capable of PCI Express Gen2 transfer rates (5 Gb/s) for a theoretical bandwidth of 20 Gb/s in each direction. This link is used to pass I/O from the SATA, SAS, LPC, and USB peripherals to the CPU or memory, along with interrupts and SMI, SCI, and SERR notification.

Universal Serial Bus (USB)

The PCH contains two Enhanced Controller Host Interface (EHCI) controllers, providing up to fourteen USB 2.0 ports. Each port allows data transfers up to 480 Mb/s. On the CPM, the following USB ports are provided:

- Port 0 – Front Panel USB0
- Port 1 – Front Panel USB1
- Port 2 – eUSB Flash 0 (Bottom Flash Module)
- Port 3 – eUSB Flash 0 (Top Flash Module)
- Port 4 – RTM Rear Panel USB
- Port 5 – H8S/2472 USB Port

The PCH provides two USB debug ports. These ports support debugger software interaction with devices on a USB 2.0 port. The USB debug port is on the front panel, USB port 1.

Serial Addressed SCSI (SAS)

The PCH provides two SAS 3G ports that are routed to the RTM for future use. The RTM must buffer the SAS signals for signal integrity.

Serial ATA (SATA)

The PCH includes two SATA host controllers that provide six SATA 3.0 ports. These ports support data transfer rates of 3.0 Gb/s. The CPM connects two SATA ports (0 and 1) for use with the optional 1.8 inch micro SATA SSD drives that can be installed in an optional Radisys DSSD MXM module.

Low Pin Count (LPC) Bridge

The Low Pin Count (LPC) bridge of the PCH provides read/write cycles for memory, I/O, DMA, and Buss Master devices. The PCH implements the LPC Interface Specification, revision 1.1. The devices contacted over this LPC bridge include the IPMI controller, the port 80 debug header, the CPU complex FPGA, and the TPM.

Serial Peripheral Interface (SPI)

The PCH provides a 4-pin SPI interface for connecting to and controlling the BIOS and ME Flash devices on the CPM. There are two 64MB Flash devices connected to the SPI bus that store BIOS boot and redundant BIOS boot code. Another 64MB Flash device contains redundant ME firmware images. On CPM power-up, the primary BIOS Flash device is selected and used. If a corrupt BIOS is detected during operation, the IPMC forces a reboot and loads the redundant BIOS Flash image.

The SPI bus allows the PCH to read and also program the primary and redundant BIOS boot Flash devices as well as the ME firmware Flash device. Controlling software as well as on-board jumpers provide Flash device write protection.

Real-Time Clock (RTC)

The PCH implements the CPM real-time clock (RTC). Rather than a battery backup, the CPM uses a 1F “SuperCapacitor” to store and supply the minimum 2V backup RTC power. As a consequence, RTC power is available for at least two hours after a system power loss.

The RTC is derived from a 32.768 KHz crystal with the following specifications:

- Frequency tolerance @ 25 °C: ± 20 ppm
- Frequency stability: maximum of -0.04 ppm/(Δ °C)^2
- Aging $\Delta F/f$ (first year @ 25 °C): ± 3 ppm
- ± 20 ppm from 0-55 °C and aging 1 ppm/year

The RTC’s capacitor-backed RAM supports two 8-byte ranges that can be locked during power loss (i.e., no read/write) when the locking bits are set. Once a range is locked, the range can be unlocked only a by a powergood reset.

SMBus/I²C bus

The PCH provides an SMBus host controller (SMBus 2.0 compliant) as well as an SMBus secondary interface. The host controller provides a mechanism for the CPU to initiate communications with SMBus peripherals (master/slave interface). The PCH also can operate in a mode that supports communication with I²C compatible devices.

The slave interface allows an external master to read from or write to the PCH. Write cycles can be used to cause certain events or pass messages and the read cycles can be used to determine the state of various status bits. The PCH internal Host Controller cannot access the internal slave Interface.

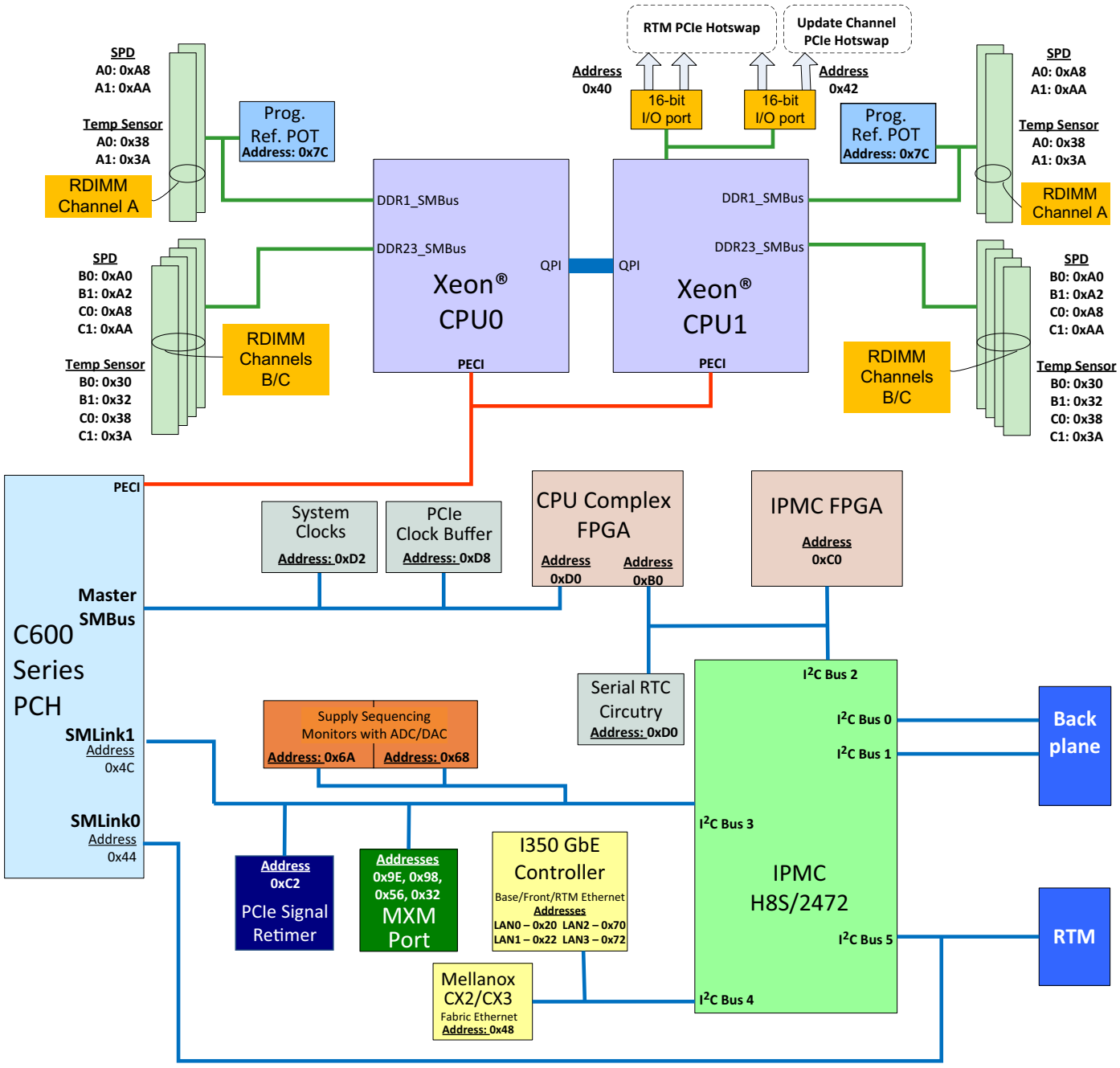
Table 8 lists the SMBus and I²C device addresses on the CPM.

Table 8. SMBus and I²C bus device addresses

Device	Bus Number	Read Address	Write Address
IPMC FPGA	IPMC I²C bus 2	C1h	C0h
CPU Complex FPGA	IPMC I²C bus 2	B1h	B0h
M41T82RM6E RTC IC	IPMC I²C bus 2	D1h	D0h
PCH SMLink0	IPMC I²C bus 5	45h	44h
PCH SMLink1	IPMC I²C bus 3	4Dh	4Ch
ADM1066	IPMC I²C bus 3	69h	68h
ADM1066	IPMC I²C bus 3	6Bh	6Ah
T0808P	IPMC I²C bus 3	C3h	C2h
MXM (possible address per spec)	IPMC I²C bus 3	33h	32h
MXM (possible address per spec)	IPMC I²C bus 3	57h	56h
MXM (possible address per spec)	IPMC I²C bus 3	99h	98h
MXM (possible address per spec)	IPMC I²C bus 3	9Fh	9Eh
I350(Base) LAN0	IPMC I²C bus 4	21h	20h
I350(Base) LAN1	IPMC I²C bus 4	23h	22h
I350(Front/RTM) LAN2	IPMC I²C bus 4	71h	70h
I350(Front/RTM) LAN3	IPMC I²C bus 4	73h	72h
CX3 (Fabric)	IPMC I²C bus 4	49h	48h
RTM MMC	IPMC I²C bus 5	GA[2:0] = GPU;	
CK420BQ	PCH Master SMBus	D3h	D2h
DB1900Z	PCH Master SMBus	D9h	D8h
CPU Complex FPGA	PCH Master SMBus	D1h	D0h

Figure 5 shows the SMBus/I²C bus mapping and lists important device addresses on the CPM.

Figure 5. ATCA-46xx SMBus/I²C bus mapping and addressing


RTM PCIe Hotswap
Update Channel PCIe Hotswap
Address 0x40
Address 0x42
16-bit I/O port
16-bit I/O port
SPD A0: 0xA8 A1: 0xAA
Temp Sensor A0: 0x38 A1: 0x3A
Prog. Ref. POT Address: 0x7C
RDIMM Channel A
DDR1_SMBus
DDR23_SMBus
QPI
Xeon® CPU0
Xeon® CPU1
PECI
SPD B0: 0xA0 B1: 0xA2 C0: 0xA8 C1: 0xAA
Temp Sensor B0: 0x30 B1: 0x32 C0: 0x38 C1: 0x3A
RDIMM Channels B/C
C600 Series PCH
Master SMBus
SMLink1 Address 0x4C
SMLink0 Address 0x44
System Clocks Address: 0xD2
PCIe Clock Buffer Address: 0xD8
CPU Complex FPGA Address 0xD0 Address 0xB0
IPMC FPGA Address 0xC0
Serial RTC Circuitry Address: 0xD0
Supply Sequencing Monitors with ADC/DAC Address: 0x6A Address: 0x68
I²C Bus 2
I²C Bus 0
I²C Bus 1
I²C Bus 3
I²C Bus 5
I²C Bus 4
IPMC H8S/2472
Back plane
RTM
Address 0xC2 PCIe Signal Retimer
Addresses 0x9E, 0x98, 0x56, 0x32 MXM Port
I350 GbE Controller Base/Front/RTM Ethernet Addresses LAN0 – 0x20 LAN2 – 0x70 LAN1 – 0x22 LAN3 – 0x72
Mellanox CX2/CX3 Fabric Ethernet Address: 0x48

Management Engine (ME)

The CPM Management Engine (ME) uses Node Manager 2.0 firmware to perform power monitoring & alert, power limiting policies, thermal monitoring & alert, and power reduction tasks during boot. As described in *Serial Peripheral Interface (SPI)* on page 30 a redundant firmware image is stored in the ME Flash in case the ME firmware needs to be recovered.

As shown in Figure 5, the IPMC I^2C Bus 5 is connected to SMLink0 on the PCH to allow the IPMC access to CPU and DIMM temperature information, PCH temperature information, CPU power information and other statistics.

IPMI controller

The IPMI controller (the IPMC) supports an "intelligent" hardware management system, based on the Intelligent Platform Management Interface Specification. The hardware management system can manage the power, cooling, and interconnect needs of intelligent devices, monitor events, and log events to a central repository.

The IPMC is a Radisys-designed reusable entity based on the Renesas H8S/2472 microcontroller and Lattice XP2 FPGA. The IPMC provides the following features:

- An external 16-bit address/data bus with internal 32-bit configuration
- Internal ROM (512KB of Flash ROM) and RAM (40KB)
- 2 MB external SPIBus-based Flash ROM
- Control of front panel LEDs (H/S, OSS, PWR, and APP)
- Monitoring of front panel Reset, and Hot Swap switching
- Control of three backplane interfaces (redundant IPMB-A/B buses and an x8 hardware address bus)
- Controller for six I^2C buses (I^2C Bus 0 - I^2C Bus 5)
- Eight analog inputs
- 8-bit parallel data bus
- Six KCS LPC address/data plus KCS LPC reset and clock interfaces
- Three serial ports (SCI-1/3/F)
- SPI bus controlled by SSC for additional Flash and FPGA support
- Eight general purpose, eight retained state, and 90 FPGA general purpose GPIO ports
- One Ethernet and one USB interface

Refer to *Appendix B, IPMI Commands and Managed Sensors,* on page 86 for more detailed information on the IPMI sensors, data, and commands.

CPU Complex (CC) FPGA

The CC FPGA module performs a number of significant monitoring and interface functions on the CPM. Many of these functions are indicated in Figure 1 on page 16. The following sections provide more details on the CC FPGA functions.

Power management and monitoring

Most of the CPM payload power supplies are monitored by two ADM1066 power sequencers, but the CC FPGA controls the power sequencing for the CPM. On power-up, it looks at the payload power enable from the IPMC to begin the power up sequence. When both power sequencers have indicated “powergood” and the external comparators indicate in-tolerance, the CC FPGA asserts PWR_OK to the PCH. The CC FPGA de-asserts PWR_OK and asserts fault signals when any monitored condition falls out-of-tolerance.

System Reset monitoring

The CC FPGA monitors the source of all Powergood, Platform, and MR-Resets and provides a 16-bit register for reset source monitoring. When the CC FPGA detects any monitored reset, it asserts an interrupt to the IPMC. The IPMC can read the reset source register and then clear the interrupt. Refer to *Reset subsystems* on page 37 for more information.

Dual UARTs, COM port, and SPI mux

Two 16550-compatible UARTs are instantiated in the CC FPGA. COM1 and COM2 ports can operate up to a 115200 baud rate (default of 115,200 baud, 8-bit, no parity, 1 stop bit). The CC FPGA is a bridge between the SPI flash programming header, the PCH and the redundant 64Mb flash devices.

The FPGA includes functionality to multiplex the internal UART connections between the front/RTM external ports and the Serial over LAN (SOL) and debug console ports from the IPMC. Refer to *Serial-Over-LAN* on page 65 for more information.

The CC FPGA is a bridge between the SPI flash programming header, the PCH and the redundant 64-Mb flash devices. Refer to *Serial Peripheral Interface (SPI)* on page 30 for more information.

LPC/I^{2}C interfaces

The CC FPGA uses an LPC interface to provide byte-wide read/write access to the internal FPGA.

I/O port 80h is used to transmit BIOS POST progress codes during boot. The CC FPGA decodes port 80 writes from the BIOS and stores the last four codes in I/O registers. The codes are shifted through the registers FIFO-style, so that the oldest code is pushed out when a new code is stored.

The CC FPGA supports dual-access to its internal I/O registers between the SMBus interface to the PCH and to IPMC I^{2}C Bus 3. An arbiter prevents data loss or corruption.

CC FPGA RTM-link

The RTM-Link relays the state of various control and status signals from a compatible programmable device on an RTM. The following signals are sent to the RTM for Ethernet LED control:

- Front Ethernet port 0 status green
- Front Ethernet port 0 status yellow
- Front Ethernet port 1 status green
- Front Ethernet port 1 status yellow

The following signals are read in from the RTM:

- RTM USB over-current (sent to the PCH)
- `SFP0 RXLOS` (Sent to I350 port 2)
- `SFP0 TX_FAULT` (Sent to I350 port 2)
- `SFP0 MOD_DEF0` (Sent to I350 port 2)
- `SFP1 RXLOS` (Sent to I350 port 3)
- `SFP1 TX_FAULT` (Sent to I350 port 3)
- `SFP1 MOD_DEF0` (Sent to I350 port 3)

Customer header configuration

All control signals configured on the customer and debug headers are routed to the CC FPGA. When any signal is in a non-default (i.e. LOW) state, a general flag bit and a state bit are set to indicate this condition. The IPMC then reads the state of these register bits as part of a normal sensor scan. The signals associated with the Customer header (P2) are:

- `CLEAR_NVRAM*`
- `SPI_WP*`
- `BIOS_RCVR_BOOT*`
- `EUSB_WP*`
- `UNR_DIS*`
- `ME Firmware Recovery`
- `FORCE BACKUP BIOS BOOT`

IPMI FPGA

The Intelligent Platform Management Interface (IPMI) Field Programmable Gate Array (FPGA) provides the specialized interfaces and glue logic needed between the H8 IPMC and rest of the CPM. The IPMC and the IPMI FPGA provide watchdog timers to help prevent the CPM from entering an unrecoverable state.

Watchdog timer 2 on the IPMI FPGA is enabled by default and starts running as soon as +3_3V_SUS power is present and the FPGA has loaded its internal flash image into its internal SRAM. If a firmware or hardware problem on the IPMC causes it to stop strobing the watchdog timer in the IPMC FPGA, it isolates the IPMC from the IPMB-A, IPMB-B, and IPMB-L buses so that they remain functional for the remaining blades in the chassis. Watchdog timer 2 then resets the IPMC.

The interfaces supported by the IPMC FPGA include the SPI bus, the I^2C bus 2, and the JTAG chain. The IPMI FPGA is programmed via the same JTAG chain as is used for the CC FPGA and any programmable devices on the RTM.

Intel I350 quad GbE Ethernet controller

The I350 has four independent network interfaces that support SerDes/SGMII or MDI (copper) protocols. The I350 has a x4 PCI Express Gen2 host interface that operates at 5.0 GT/s and is capable of negotiating to x2 and x1 link widths. The I350 provides virtualization support including PCI-SIG Single-Root I/O Virtualization, VMDq2 support for up to eight virtual machines and eight TX and RX queues per port. The I350 has NC-SI and SMBus interfaces that support pass-through traffic for Serial-Over-LAN (SOL) support from the IPMC. The CPM has both interfaces connected to allow flexibility for the IPMI code development. Initial configuration information for the controller (including management setup and SMBus addresses) is provided via a 256Kb SPI EEPROM, which is read upon power-up.

Mellanox dual 40GbE controller

The CPM provides two 40GbE ports using a Mellanox ConnectX-3 (CX3) controller. The CX3 is connected to a x8 Gen 3 PCI Express port that provides a peak data bandwidth of 64Gb/s in each direction. The CX3 has two integrated Gigabit Ethernet MAC/PHY ports that support the following standard Ethernet interfaces for CPM:

- 40GBASE-KX4 (IEEE 802.3ba)
- 10GBASE-KX4 (IEEE 802.3ap)
- 1000BASE-KX (IEEE 802.3ap)

The CX3 has a flash boot interface and the CPM uses a 32Mb flash device to store boot firmware and configuration options for the controller. The CX3 supports PCI-SIG SR-IOV, providing up to 128 virtual machines.

The CX3 controller is used to connect to Fabric Channels 1 and 2 on the Zone 2 connector. The TX pairs connect directly to the connector while the RX pairs have DC blocking caps between the controller and the connector.

The CX3 has iSCSI and PXE boot support enabled in the SPI flash firmware. iSCSI and PXE cannot be enabled at the same time; the desired function must be selected in the BIOS setup menu.

Clock synthesizer subsystem

CPM uses two major components, a CK420BQ and a DB1900Z to generate the clock signals used by the CPUs, by the PCH, and by other peripheral components.

The CK420BQ clock generator provides host, chipset, PCI and LPC peripheral clocks on the CPM. The device uses a 25.0000 MHz reference crystal and receives control input from the BIOS over the SMBus. The clock signals are supplied to the CPUs, the PCH, the TPM, the IPMC, and the CC FPGA.

The DB1900Z differential buffer distributes 100MHz clocks to the PCI Express and QPI devices. The clocks output by this device are based on a reference clock from the CK420BQ clock generator. In addition to the PCIe and QPI clocks, this device supplies reference clocks for the Mellanox CX2/CX3 and Intel I350 GbE controllers, the RTM PCIe interfaces, and the MXM connector.

In addition to the above reference clocks, the following oscillators or crystals are provided on the CPM:

- A 40.000 MHz 100ppm oscillator is provided for the CC FPGA.
- The CC FPGA provides a 6.6 MHz clock for the RTM-L interface to the RTM.
- A 32.768 kHz crystal is provided for the PCH RTC.
- A 32.768 kHz crystal is provided for the IPMC RTC.
- A 32.768 kHz crystal is provided for the Trusted Platform Module.
- A 25.000 MHz 30ppm crystal is provided for the CK420BQ
- A 25.000 MHz 30ppm crystal is provided for the I350 quad GbE controller
- A 32.000 MHz 50ppm oscillator is provided for the IPMC FPGA
- A 156.25 MHz 50ppm oscillator is provided for the Mellanox CX3 40G Ethernet controller

Reset subsystems

CPM9 supports three types of reset: platform reset, powergood reset, and memory-retained (MR) reset.

Platform reset

A platform reset (the PLTRST* signal) is defined as a total system board reset (except for IPMI circuitry). All devices and registers are reset to their default state. After a platform reset all data in DRAM may be invalid due to the CPU memory controller discontinuing refresh cycles. Memory is then cleared during the system BIOS initialization.

The platform reset signal originates in the PCH. The potential sources or triggers of a platform reset include:

- The front panel Reset button
- A reset assertion generated over the board debug header during a troubleshooting session
- An IPMC reset command generated due to one of the following events:
  - Watchdog timer expiration
  - An MR reset is asserted (by either the PCH or the IPMC) but they are disabled in the CC FPGA. In this case it reverts to a platform reset.

Powergood reset

A powergood reset is similar to a platform reset, except that all sticky bits in the CPU and PCH are cleared. For the CPUs, a powergood reset will result in reset of all the states in the processor, including the sticky state that is preserved on the other resets.

There is a “Powergood Reset” enable bit in the reset control register of the CC FPGA. When this bit is set, all platform resets are converted to Powergood resets. In other words, when this bit is set, any of the sources or triggers that would otherwise cause a platform reset will instead cause a powergood reset.

There is a second enable bit in the CC FPGA, that when set also asserts Powergood Reset, normally from the BIOS.

Memory-Retained (MR) reset

A memory-retained reset will preserve the contents of main memory while the rest of the system experiences a Platform Reset. The intended usage for MR-Reset is to provide an operating system kernel crash dump location, so that debug information can be recovered after an OS crash.

When an MR-Reset is initiated from one of the sources, the result is an INIT* virtual legacy wire (VLW) message sent to the CPUs from the PCH. INIT* triggers the BIOS to run from the reset vector in the shadowed F000 segment, where the MR-Reset code is stored. If a valid signature exists in this location (i.e. MR-Reset has been enabled in the BIOS setup menu) then the MR-Reset code is executed. The INIT* sequence has PCH drive the INIT* VLW message to the CPUs and the INIT_3_3V* signal to the CC FPGA.

The MR-Reset BIOS code puts the system into the S3 sleep state. In S3, the internal memory controller for each CPU places all the DIMMs on the associated memory channels into self-refresh and the PCH asserts the PLTRST* signal. The RTC alarm in the PCH is used to wake the system up from S3, causing the PCH to de-assert PLTRST*. The BIOS uses the S3 resume path and skips over memory initialization. This method allows the contents of the DIMMs to remain valid while the system is reset.

Table 9 lists the potential sources/triggers for the MR-Reset. Though similar, these sources are slightly different from those for a platform or powergood reset.

Table 9. Memory-Retained Reset Sources

Platform Reset Source	Description
Front panel Reset button (FP_RESET*)	Pushing the button triggers an RCIN* assertion to the PCH, thus beginning the INIT* sequence.
RTM reset push button	The RTM MMC sends OEM command to IPMC. Upon receiving the “warm reset” OEM command, the IPMC asserts IPMC_MR_RESET*
IPMC warm reset command (IPMC_COLD_RESET*)	One of the following two triggers are detected by the IPMC: • Watchdog timer 1 is configured for warm reset and times out. • The IPMC warm reset command is recognized. Once one of the above triggers are detected, the IPMC_MR_RESET* signal is asserted to the CC FPGA which triggers an RCIN* assertion to the PCH, thus beginning the INIT* sequence.

Watchdog timers

The CPM uses a number of watchdog timers to prevent the board from entering an unrecoverable state. The IPMC and the IPMC FPGA provide the following watchdog timers:

- Corrupt Flash detection watchdog
- OS watchdog timer (Watchdog 1)
- IPMC watchdog timer (Watchdog 2)

The following sections describe the operations performed by each watchdog.

Corrupt Flash detection watchdog

The Corrupt Flash Detection (CFD) Watchdog is a SW-based watchdog that allows the CPM to recover when the primary SPI flash is either blank or the boot block is corrupted. The CFD watchdog timer is started any time that a reset is asserted to the payload processor (for example, platform reset, push button reset, and so on). Responsibility is then passed to the system BIOS to disable the timer. If the timer is not disabled before it expires, the IPMC firmware:

1. Disables payload power,
2. Selects the secondary boot flash using the Boot Flash Select Control, and then
3. Re-enables payload power to boot from the secondary SPI flash.

OS watchdog timer (Watchdog 1)

This programmable watchdog is used with the BIOS and the Linux OS. It can be used by any OS.

IPMC watchdog timer (Watchdog 2)

The IPMC FPGA includes a hardware watchdog timer, Watchdog 2. This watchdog is enabled by default and will start running as soon as +3_3V_SUS power is present and the FPGA has loaded its internal flash image into its internal SRAM. The default timeout on power-up is 10 seconds. After the IPMC boot-loader is finished, the IPMC reprograms the timeout for 6 seconds and will continue to strobe every 2 seconds. If a firmware or hardware problem on the IPMC causes it to stop strobing the watchdog timer in the IPMC FPGA:

1. The IPMC is automatically isolated from the IPMB-A, IPMB-B and IPMB-L buses so that they remain functional for the remaining blades in the chassis,
2. Watchdog 2 forces a reset of the IPMC.

Power subsystems

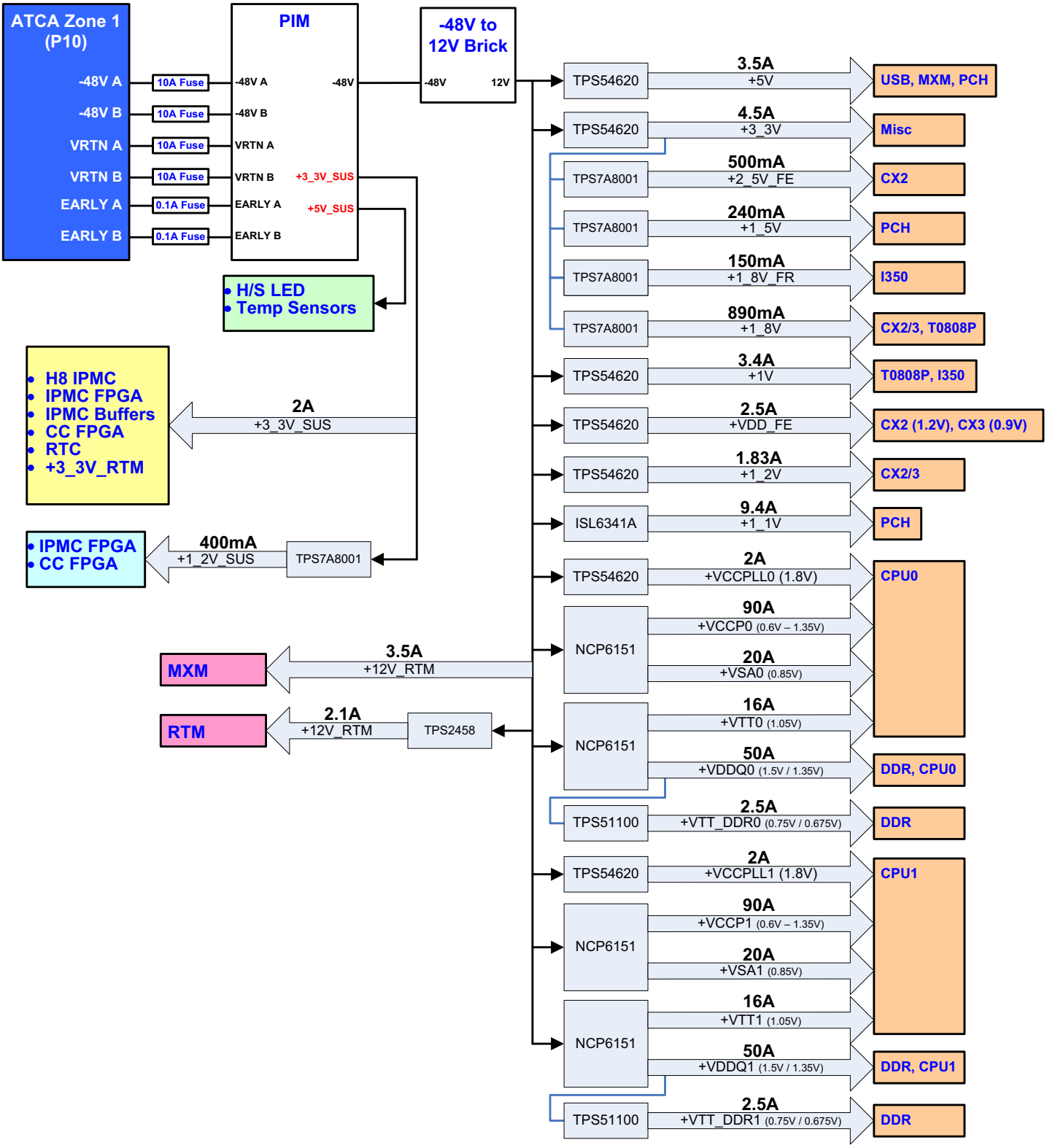
All CPM power is supplied through the P10 backplane connector as -48VDC, as specified by the PICMG 3.0 specification. The use of DC power minimizes the possibility of RFI and EMI interference for the on-board and board-to-board signals in ATCA components. Figure 6 shows the power architecture and distribution for the CPM.

Input protection and monitoring

Each of the main power feeds (-48 A/B) and return feeds (VRTN A/B) of the CPM is protected by a 10A fast-blow fuse. This protects the CPM circuitry in the event power draw exceeds the rated 350W power by a significant amount. In addition, the ENABLE_A/B inputs to the power input module (PIM) are each protected by 100 mA fuses.

The CPM does not monitor input voltage directly, but the IPMC does detect input voltage presence at the Zone 1 connector and compares it with the PIM_STATUS signal. Any status difference indicates one or more input fuses have blown.

Figure 6. ATCA-46xx Power Subsystem



Power Input Module (PIM)

A power input module (PIM) between the input fuses and main power brick (-48V to 12V supply) provides input power conditioning and the following additional features:

- Current handling up to 300W
- Inrush current limit protection
- Integrated filter designed to meet CISPR class B EMI limits
- 11.88W of isolated auxiliary 3.3V power for IPMI circuitry.
- 750mW of isolated auxiliary 5V power for IPMI circuitry.
- ORing FETs on A and B –48V feeds
- A/B feed loss alarm
- Hot-swap control
- Glitch hold-up circuit based on external capacitor and 72V charging circuit
- Input under voltage and over voltage protection
- Over current and thermal protection

In addition to the above features, the PIM incorporates circuitry to charge external voltage-hold capacitors. These external capacitors (1100uF/100V) charge to a nominal 72V and provide short-term transient and power loss protection in support of PICMG 3.0 requirements.

Two internal PIM regulators (a 3.3V switching supply and a 5V linear supply) send power to IPMC components, the FPGAs, RTC circuitry, the RTM, H/S LEDs, and temperature sensors.

Payload power supplies

The main power supply (an isolated quarter brick DC-DC convertor; the brick) is a -48V to 12V convertor. It supplies all of the +12VDC power for the CPM. With the exception of the +3.3V and +5V output from the PIM, all other voltages on the CPM and RTM either come directly from or are converted from the +12V outputs of this brick. Refer to Figure 6 for detailed information on the DC-DC convertors that connect to the brick output, the voltages/current developed, and the CPM devices that individual payload power supplies feed.

Trusted Platform Module (TPM)

The CPM uses an Infineon SLB9635TT1.2 Trusted Platform Module (TPM) to implement version 1.2 of the Trusted Computing Group specification. The TPM sits on the LPC bus and has the ability to assert an interrupt through the PCH Serial IRQ interface.

The TPM is a secure key generator and key cache management device that supports industry standard cryptographic APIs. The TPM contains sufficient cryptographic functionality to generate, store, and manage cryptographic keys in hardware while leveraging the resources of the rest of the system platform.

The five major functions of the TPM are:

- Public key functions for on-chip key pair generation using a hardware RNG

- Public key signature, encryption, and decryption to enable secure storage of data and digital secrets
- Storage of hashes (unique numbers calculated from pre-runtime configuration information) that enable verifiable attestation of the machine configuration when booted
- An endorsement key that can be used to anonymously establish that an identity key was generated in a TPM.
- Initialization and management functions that allow the owner to turn TPM functionality on and off, reset the chip, and take ownership of its functions

MXM type A video module (optional)

The CPM includes support for an optional Type A MXM 3.0 module. Due to the limited board height available with ATCA CPM boards, the fan or heat sink for standard MXM video modules cannot be used with the ATCA-46xx CPM. Contact Radisys Technical Support for help with a heat sink solution for any selected Type A MXM 3.0 video module.

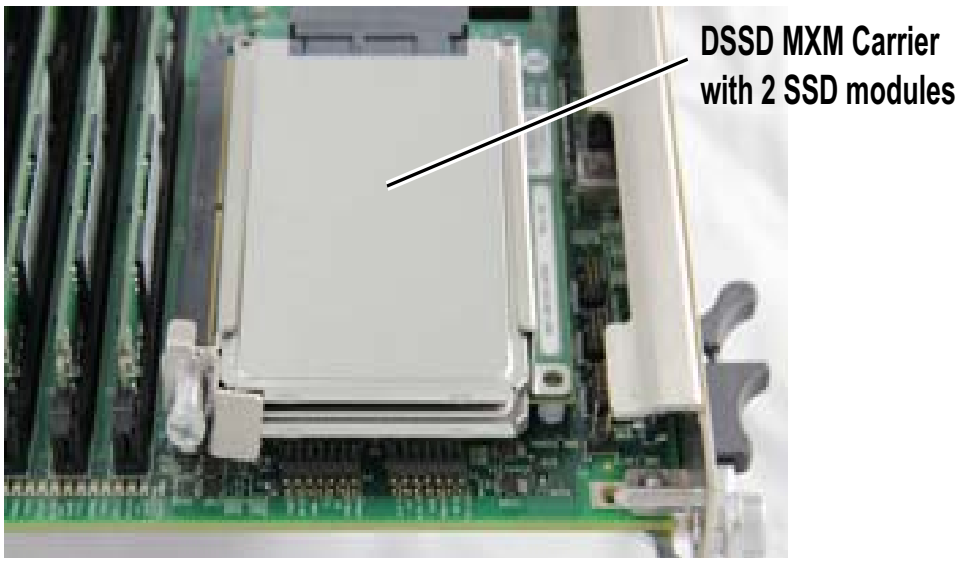
The MXM site supports DisplayPort digital video signaling to the front panel and also connects to the x16 PCI Express port from CPU0 (port 3).

1.8” Solid State Drive (SSD) module (optional)

The CPM supports installation of one or two 6 Gbps microSATA SSD drives installed in an optional carrier module that mounts and connects to the board MXM port. Figure 7 shows the ATCA-46xx CPM with a mounted DSSD MXM carrier module that has two microSATA SSD drives installed.

The DSSD MXM carrier module usually ships separately, and includes a sheet with assembly and installation instructions.

Figure 7. DSSD MXM carrier module



eUSB Embedded Flash module (optional)

The CPM supports up to two embedded USB (eUSB) NAND Flash modules. The modules are USB 2.0 compliant and currently provide sizes from 1GB to 32GB of SLC NAND Flash. The eUSB modules have read speed support of up to 35MB/s and write speed up to 17MB/s. Figure 8 shows an eUSB NAND Flash module ready for installation on the ATCA-46xx CPM.

Figure 8. eUSB NAND Flash module

The modules are stackable with a “Bottom” version form factor that passes through a USB connection to a “Top” form factor module, providing redundant flash drive support in a small footprint. The CPM uses PCH USB ports 2 and 3 for the eUSB modules.

Chapter 3

Software/Firmware Description

Introduction

The CPM has the following software and firmware associated with it:

- The system BIOS
- The IPMI firmware
- Software/firmware update support software
- Operating system support software

The following sections provide more information.

System BIOS

The system BIOS is designed on a base source code licensed from American MegaTrends Inc. (AMIBIOS) and is adapted to meet the requirements of the ATCA-46xx CPM. The system BIOS is an implementation of the Unified Extensible Firmware Interface (UEFI) specification 2.1 as published by the UEFI forum (www.uefi.com).

System BIOS features

The CPM system BIOS has the following features:

- CPM boot time in less than 30 seconds excluding extended memory and option ROM initialization requirements
- Source code based on UEFI specification
- Support for the processor and PCH features of the CPM as well as all major board features
- User configurable through the BIOS Setup utility

BIOS setup menus

The system BIOS contains a setup utility for modifying the system configuration. The system configuration information is maintained in the redundant boot flash devices and is used by the system BIOS to initialize the hardware.

Access to the setup menus is available for only a short time during the boot process. Pressing **F2** during boot enables access to the setup utility. The **Delete** key is an alternative that works in some situations when **F2** does not.

The BIOS setup menus include standard menus and additional custom menus from Radisys. A legend on the right side of each menu provides navigation and selection information.

Table 10 gives a general overview of the BIOS setup menu hierarchy.

Table 10. BIOS setup menu hierarchy.

Top-Level Menu	Information Items and Sub-Menus	
Main, Table 11 on page 46	• BIOS Information • System Language	• Memory Information • Access Level
Advanced, Table 12 on page 47	• PCI Subsystem Settings • Trusted Computing • CPU Configuration • Legacy OpROM Control • SAS Configuration • USB Configuration • Serial Port Console Redirection	• ACPI Settings • WHEA Configuration • Runtime Error Logging • SATA Configuration • Thermal Configuration • Super I/O Configuration
Chipset, Table 13 on page 53	• North Bridge Settings • ME Subsystem Settings	• South Bridge Settings
IPMI, Table 14 on page 56	• System Event Log Settings	• View System Information
Boot (Table 15 on page 57)	• Boot Configuration	• Boot Option Priorities
Security (Table 15)	• Security password (Administrator)	• Security password (User)
Save & Exit (Table 15)	• Save and Exit options • Restore Defaults	• Save options • Boot Override

Table 11 lists the Radisys default settings for the Main menu of the CPM BIOS setup.

Table 11. Radisys default BIOS Main menu setup options

Main menu		
Submenu	Setup Item	Values [Default]
BIOS Information	BIOS Vendor	[Dynamic update]
	Core Version	[Dynamic update]
	Compliancy	[Dynamic update]
	Project Version	[Dynamic update]
	Build Date and Time	[Dynamic update]
Memory Information	Total Memory	[Dynamic update]
	System Language	[*English*]
	Engineering Mode	*Enabled* [*Disabled*]
	Access Level *User*	User defined
	Access Level *Administrator*	User defined

Note: The Radisys default setting for each of the above BIOS setup options is indicated with square brackets ([ ]) surrounding the option or the required entry. If multiple choices are available for a menu item, each choice is indicated in *italics*. If there are no required settings for a menu item, that item does not appear in this table.

Table 12 lists the Radisys default settings for the Advanced menu of the CPM BIOS setup.

Table 12. Radisys default BIOS Advanced menu setup options

Advanced Menu		
Submenu	Setup Item	Values [Default]
Top level: Advanced Menu	Front/Rear Ethernet	[*EEPROM Setting*] *Front/Copper* *Rear/SGMII* *Rear/SERDES*
	Spread Spectrum	[*Enabled*] *Disabled*
	SOL Priority port	[*FRONT/Serial Port 0*] *REAR/Serial Port 1*
PCI Subsystem Settings: Top Level	PCI Bus Driver Version	[Dynamic update]
	PCI Option ROM Handling: PCI ROM Priority	*Legacy ROM* [*EFI Compatible ROM*]
	PCI 64bit Resources Handling: Above 4G Decoding	*Enabled* [*Disabled*]
	PCI Common Settings: PCI Latency Timer	[*32 PCI Bus Clocks*] *64 PCI Bus Clocks* *96 PCI Bus Clocks* *128 PCI Bus Clocks* *160 PCI Bus Clocks* *192 PCI Bus Clocks* *224 PCI Bus Clocks* *248 PCI Bus Clocks*
	PCI Common Settings: VGA Palette Snoop	*Enabled* [*Disabled*]
	PCI Common Settings: PERR# Generation	*Enabled* [*Disabled*]
	PCI Common Settings: SERR# Generation	*Enabled* [*Disabled*]
PCI Subsystem Settings: PCI Express Settings	PCI Express Device Register Settings: Relaxed Ordering	*Enabled* [*Disabled*]
	PCI Express Device Register Settings: Extended Tag	*Enabled* [*Disabled*]
	PCI Express Device Register Settings: No Snoop	[*Enabled*] *Disabled*
	PCI Express Device Register Settings: Maximum Payload	[*Auto*] *128 Bytes* *256 Bytes* *512 Bytes* *1024 Bytes* *2048 Bytes* *4096 Bytes*
	PCI Express Device Register Settings: Maximum Read Request	[*Auto*] *128 Bytes* *256 Bytes* *512 Bytes* *1024 Bytes* *2048 Bytes* *4096 Bytes*
	PCI Express Link Register Settings ASPM Support	[*Disabled*] *Auto* *Force L0s*
	PCI Express Link Register Settings Extended Synch	*Enabled* [*Disabled*]
	PCI Express Link Register Settings Link Training Retry	*Disabled* *2* *3* [*5*]
	PCI Express Link Register Settings Link Training Timeout (uS)	[*100*]
	PCI Express Link Register Settings Unpopulated Links	[*Keep Link ON*] *Disable Link*

Table 12. Radisys default BIOS Advanced menu setup options (continued)

Advanced Menu		
Submenu	Setup Item	Values [Default]
PCI Subsystem Settings: PCI Express GEN2 Settings	PCI Express GEN2 Device Register Settings Completion Timeout	[*Default*] *Shorter Longer Disabled*
	PCI Express GEN2 Device Register Settings ARI Forwarding	*Enabled* [*Disabled*]
	PCI Express GEN2 Device Register Settings AtomicOp Req Enable	*Enabled* [*Disabled*]
	PCI Express GEN2 Device Register Settings AtomicOp Egress Block	*Enabled* [*Disabled*]
	PCI Express GEN2 Device Register Settings IDO Request Enable	*Enabled* [*Disabled*]
	PCI Express GEN2 Device Register Settings IDO Completion Enable	*Enabled* [*Disabled*]
	PCI Express GEN2 Device Register Settings LTR Mechanism Enable	*Enabled* [*Disabled*]
	PCI Express GEN2 Device Register Settings E2E TLP Prefix Block	*Enabled* [*Disabled*]
	PCI Express GEN2 Link Register Settings Target Link Speed	[*Auto*] *Force to 2.5 GT/s* *Force to 5.0 GT/s*
	PCI Express GEN2 Link Register Settings Clock Power Management	*Enabled* [*Disabled*]
	PCI Express GEN2 Link Register Settings Compliance SOS	*Enabled* [*Disabled*]
	PCI Express GEN2 Link Register Settings HW Autonomous Width	[*Enabled*] *Disabled*
	PCI Express GEN2 Link Register Settings HW Autonomous Speed	[*Enabled*] *Disabled*
PCI Subsystem Settings: PCI Hot-Plug Settings	BIOS Hot-Plug Support	[*Enabled*] *Disabled*
	PCI Buses Padding	*Disabled* [*1*] *2 3 4 5*
	I/O Res Padding	*Disabled* [*4 K*] *8 K 16 K 32 K*
	MMIO32 Res Padding	*Disabled 1 M 2 M 4 M 8 M* [*16 M*] *32 M 64 M 128 M*
	PFMMIO32 Res Padding	*Disabled 1 M 2 M 4 M 8 M* [*16 M*] *32 M 64 M 128 M*
	MMIO64 Res Padding	[*Disabled*] *1 M 2 M 4 M 8 M 16 M 32 M 64 M 128 M 256 M 512 M 1 G*
	PFMMIO64 Res Padding	[*Disabled*] *1 M 2 M 4 M 8 M 16 M 32 M 64 M 128 M 256 M 512 M 1 G*
ACPI Settings	ACPI Auto Config	*Enabled* [*Disabled*]
	Enable Hibernation	[*Enabled*] *Disabled*
	Lock Legacy Resources	*Enabled* [*Disabled*]

Table 12. Radisys default BIOS Advanced menu setup options (continued)

Advanced Menu		
Submenu	Setup Item	Values [Default]
Trusted Computing Settings: Configuration	Security Device Support	*Enabled* [*Disabled*]
	TPM State	*Enabled* [*Disabled*]
	Pending operation	[*None*] *Enable Take Ownership* *Disable Take Ownership* *TPM Clear*
	Security Device Support	*Enabled* [*Disabled*]
	TCM State	*Enabled* [*Disabled*]
	Pending operation	[*None*] *Enable Take Ownership* *Disable Take Ownership* *TPM Clear*
Trusted Computing Settings: Current Status Information	TPM Enabled Status:	*Enabled* [*Disabled*]
	TPM Active Status:	[*Deactivated*] *Activated*
	TPM Owner Status:	*Owned* [*Unowned*]
	TPM Enabled Status:	*Enabled* [*Disabled*]
	TPM Active Status:	[*Deactivated*] *Activated*
	TPM Owner Status:	*Owned* [*Unowned*]
WHEA Configuration	WHEA Support	[*Enabled*] *Disabled*
CPU Configuration	Socket 0	[Dynamic update]
	Socket 1	[Dynamic update]
	CPU Speed	[Dynamic update]
	64-bit	[Dynamic update]
	Mismatch CPU	[Dynamic update]
	Hyper-threading	[*Enabled*] *Disabled*
	Active Processor Cores	[*All*] *1 2 3 4 5 6 7 8 9*
	Limit CPUID Maximum	*Enabled* [*Disabled*]
	Execute Disable Bit	[*Enabled*] *Disabled*
	Hardware Prefetcher	[*Enabled*] *Disabled*
	Adj CacheLine Prefetch	[*Enabled*] *Disabled*
	DCU Streamer Prefetcher	[*Enabled*] *Disabled*
	DCU IP Prefetcher	[*Enabled*] *Disabled*
	Data Reuse Optimization	[*Enabled*] *Disabled*
	Intel Virtualization Technology	[*Enabled*] *Disabled*
	Local APIC Mode	[*Auto*] *x2APIC* *xAPIC*
CPU Configuration: Socket 0/1 CPU Information	CPU Signature	[Dynamic update]
	Microcode Patch	[Dynamic update]
	Max CPU Speed	[Dynamic update]
	Min CPU Speed	[Dynamic update]
	Processor Cores	[Dynamic update]
	Intel HT Technology	[Dynamic update]
	Intel VT-x Technology	[Dynamic update]
	L1 Data Cache	[Dynamic update]
	L1 Code Cache	[Dynamic update]
	L2 Cache	[Dynamic update]
	L3 Cache	[Dynamic update]

Table 12. Radisys default BIOS Advanced menu setup options (continued)

Advanced Menu		
Submenu	Setup Item	Values [Default]
CPU Configuration: CPU Power Management Configuration	Power Technology	[*Disable*] *Energy Efficient* *Custom*
	EIST	*Enabled* [*Disabled*]
	Turbo Mode	*Enabled* [*Disabled*]
	P-STATE Coordination	[*HW_ALL*] *SW_ALL* *SW_ANY*
	CPU C3 Report	*Enabled* [*Disabled*]
	CPU C6 report	*Enabled* [*Disabled*]
	CPU C7 report	*Enabled* [*Disabled*]
	Package C State limit	*C0 C1 C2 C3 C6 C7* [*No Limit*]
	Energy Performance	*Performance* [*Balanced Performance*] *Balanced Energy* *Energy Efficient*
	Factory long duration power limit	[Dynamic update] (Watts)
	Long duration power limit	[*0*]
	Factory long duration maintained	[Dynamic update] (Time)
	Long duration maintained	[*0*]
	Recommended short duration power limit	[*1.2 * Long Duration*] (Watts)
	Short duration power limit	[*0*]
	Base Frequency	[Dynamic update] (MHz)
	[*1 2 3 4 5 6 7 8*]-Core Ratio Limit	[*0*] *0* uses the factory-configured value for the *n-Core Ratio Limit* value.
Runtime Error Logging	Runtime Error Logging Support	[*Enabled*] *Disabled*
	Mem Err Threshold	[*10*]
	Max Mem Err Events	[*10*]
	PCI Error Logging	*Enabled* [*Disabled*]
	Poison Support	*Enabled* [*Disabled*]
	Poison Support in IOH	*Enabled* [*Disabled*]
	DMI Error Logging	*Enabled* [*Disabled*]
Legacy OpROM Control	Launch Network OpROM	[*Enabled*] *Disabled*
	Fabric 10/40G OpROM	[*Enabled*] *Disabled*
	Front/Rear GbE OpROM	*Disabled* [*PXE*] *iSCSI*
	Base GbE OpROM	*Disabled* [*PXE*] *iSCSI*
	Launch Storage OpROM	[*Enabled*] *Disabled*
	Onboard SAS OpRom	*Enabled* [*Disabled*]
	Onboard SATA RAID OpRom	[*Enabled*] *Disabled*
	Launch RTM OpROM	[*Enabled*] *Disabled*

Table 12. Radisys default BIOS Advanced menu setup options (continued)

Advanced Menu		
Submenu	Setup Item	Values [Default]
SATA Configuration	SATA Port[*0 1*]	[Dynamic update]
	SATA Mode	*Disabled IDE Mode* [*ACHI Mode*] *RAID Mode*
	Serial-ATA Controller 0	*Disabled Enhanced* [*Compatible*]
	Serial-ATA Controller 1	[*Disabled*] *Enhanced*
	Aggressive Link Power Management	*Enabled* [*Disabled*]
	Port [*0 1 2 3 4 5*] Hot Plug	*Enabled* [*Disabled*]
	External SATA Port [*0 1 2 3 4 5*]	*Enabled* [*Disabled*]
	Staggered Spin-up (SATA Port [*0 1 2 3 4 5*])	*Enabled* [*Disabled*]
SAS Configuration	SAS Port [*0 1 2 3 4 5 6 7*]	[Dynamic update] Based on detected SAS devices.
Thermal Configuration	Thermal Management	[*Enabled*] *Disabled*
	ME SMBus Therm Report	[*Enabled*] *Disabled*
	PCH Temp Read	[*Enabled*] *Disabled*
	CPU Energy Read	[*Enabled*] *Disabled*
	CPU Temp Read	[*Enabled*] *Disabled*
	Alert Enable Lock	*Enabled* [*Disabled*]
	PCH Alert	*Enabled* [*Disabled*]
	DIMM Alert	*Enabled* [*Disabled*]
USB Configuration: USB Devices:	USB Devices:	[Dynamic update] Based on detected USB devices.
	USB Support	[*Enabled*] *Disabled*
	Legacy USB Support	[*Enabled*] *Disabled Auto*
	EHCI Hand-off	*Enabled* [*Disabled*]
	Port 60/64 Emulation	[*Enabled*] *Disabled*
USB Configuration: USB hardware delays and time-outs:	USB transfer time-out	*1 sec 5 sec 10 sec* [*20 sec*]
	Device reset time-out	*10 sec* [*20 sec*] *30 sec 40 sec*
	Device power-up delay	[*Auto*] *Manual*
	Device power-up delay in seconds	[*5*] 1 - 40 second range
	Mass Storage Devices: (The text is updated dynamically)	[*Auto*] *Floppy Forced FDD* *Hard Disk CD-ROM*
Super IO Configuration: Serial Port 0/1 Configuration	Serial Ports (The text is updated dynamically) System Serial Port Parameters.	Radisys FPGA
	Serial Port	[*Enabled*] *Disabled*
	Device Settings	[Dynamic update] Reset required.
	Change Settings	[*Auto*] *IO=3F8h; IRQ=4;* *IO=3F8h; IRQ=3,4,5,6,7,10,11,12;* *IO=2F8h; IRQ=3,4,5,6,7,10,11,12;* *IO=3E8h; IRQ=3,4,5,6,7,10,11,12;* *IO=2E8h; IRQ=3,4,5,6,7,10,11,12;*

Table 12. Radisys default BIOS Advanced menu setup options (continued)

Advanced Menu		
Submenu	Setup Item	Values [Default]
Serial Port Console Redirection	COM0: Console Redirection	[*Enabled*] *Disabled* [Dynamic update] if port is disabled.
	COM1: Console Redirection	*Enabled* [*Disabled*] [Dynamic update] if port is disabled.
Serial Port Console Redirection: Redirection Via AMI Debugger	Console Redirection Engineering mode.	[*Enabled*] *Disabled*
	Terminal Type	*VT100* [*VT100+*] *VT-UTF8 ANSI*
	Serial Port for Out-of-Band Management Windows Emergency Management Services (EMS)	Engineering mode
Serial Port Console Redirection: COM 0/1 Console Redirection Settings	Out-of-Band Mgmt Port	[*COM0*] *COM1*
	Terminal Type	*VT100* [*VT100+*[a]] [*VT-UTF8*[b]] *ANSI*
	Bits per second	*9600 19200 38400 57600* [*115200*]
	Flow Control	[*None*] *Hardware RTS/CTS Software Xon/Xoff*
	Data Bits	*7* [*8*]
	Parity	[*None*] *Even Odd Mark Space*
	Stop Bits	[*1*] *2*
	Flow Control	[*None*] *Hardware RTS/CTS*
	VT-UTF8 Combo Key Support	[*Enabled*] *Disabled*
	Recorder Mode	*Enabled* [*Disabled*]
	Resolution 100x31	*Enabled* [*Disabled*]
	Legacy OS Redirection Resolution	[*80x24*] *80x25*
	Putty KeyPad	[*VT100*] *LINUX XTERMR6 SCO ESCN VT400*

Note: The Radisys default setting for each of the above BIOS setup options is indicated with square brackets ([ ]) surrounding the option or the required entry. If multiple choices are available for a menu item, each choice is indicated in *italics*. If there are no required settings for a menu item, that item does not appear in this table.
[a]Default for COM0/COM1.
[b]Default for out-of-band management port.

Some configuration settings can result in hardware conflicts. It is important to understand the hardware configuration and resource needs to prevent conflicts.

Table 13 lists the Radisys default settings for the Chipset menu of the CPM BIOS setup..

Table 13. Radisys default BIOS Chipset menu setup options

Chipset Menu		
Submenu	Setup Item	Values [Default]
North Bridge, Memory Configuration	Total Memory	[Dynamic update]
	Current Memory Mode	[Dynamic update]
	Current Memory Speed	[Dynamic update]
	Mirroring	[Dynamic update]
	Sparing	[Dynamic update]
	Spare Err Threshold	[*15*]
	DRAM RAPL BWLIMIT	*0 [1] 8 16*
	Perfmon and DFX devices	[*HIDE*] *UNHIDE*
	DRAM RAPL MODE	*Disabled DRAM RAPL MODE0* [*DRAM RAPL MODE1*]
	Numa	[*Enabled*] *Disabled*
	DDR3 Refresh Policy	*1X Refresh [2X Refresh*]
	Mem bandwidth throttling	*Enabled* [*Disabled*]
	Memory ECC	[*Enabled*] *Disabled*
	Memory VDD	*Energy Saving* [*Max Performance*]
	Oppor. CKE Power-Down	[*Disabled*] *APD ON, PPD OFF APD OFF, PPD Fast APD OFF, PPD Slow APD ON, PPD Fast APD ON, PPD Slow*
	Self-Refresh	*Enabled* [*Disabled*]
	MPST Support	*Enabled* [*Disabled*]
	DDR Speed Limit	*Auto Force DDR3 800 Force DDR3 1066 Force DDR3 1333* [*Force DDR3 1600*] *Force DDR3 1866*
	Channel Interleaving	[*Auto*] *1 Way 2 Way 3 Way 4 Way*
	Rank Interleaving	[*Auto*] *1 Way 2 Way 4 Way 8 Way*
	Patrol Scrub	[*Enabled*] *Disabled*
	Demand Scrub	[*Enabled*] *Disabled*
	Data Scrambling	*Enabled* [*Disabled*]
	Rank Margin	*Enabled* [*Disabled*]
	Thermal Throttling	*Disabled OLTT* [*CLTT*]
	OLTT Peak BW %	*25 ...* [*50*] *...100*
	Altitude	*Auto* [*300 M*] *900 M 1500 M 3000 M*
	Serial Message Debug Level	[*Minimum*] *Maximum Trace Memory Training*

Table 13. Radisys default BIOS Chipset menu setup options (continued)

Chipset Menu		
Submenu	Setup Item	Values [Default]
North Bridge, IOH Configuration	Intel(R) I/OAT	*Enabled* [*Disabled*]
	DCA Support	[*Enabled*] *Disabled*
	VGA Priority	Onboard / [Offboard*]
	TargetVGA	*CPU 0* [*Dynamic update*]
	Gen3 Equalization WA's	*Enabled* [*Disabled*]
	Gen3 Equalization Fail WA	*Enabled* [*Disabled*]
	Gen3 Equalization Phase 2/3 WA	*Enabled* [*Disabled*]
	Equalization Phase 2/3 Supported	*Enabled* [*Disabled*]
	Gen3 Equalization Redoing WA	*Enabled* [*Disabled*]
	IOH Res Selection Type	[*Auto*] *Manual*
	MMIOH Size	*1G 2G 4G 8G 16G 32G* [*64G*] *128G*
	MMCFG BASE	[*0x80000000*] *0xA0000000 0xC0000000*
	Io Ratio Skt0	*1* ... [*3*] ... *8*
	Io Ratio Skt1	*1* ... [*2*] ... *8*
	Mmio Ratio Skt0	*1* ... [*6*] ... *8*
	Mmio Ratio Skt1	*1* ... [*2*] ... *8*
North Bridge, IOH Configuration CPU 0/1 PCIe port Bifurcation Control	PORT 1A/B Link Speed	*GEN1* [*GEN2*] *GEN3*
	PORT 2A/B/C/D Link Speed	*GEN1* [*GEN2*] *GEN3*
	PORT 3A/B/C/D Link Speed	*GEN1* [*GEN2*] *GEN3*
	CPU 1 PORT 3A/B Link Speed	[*GEN1*] *GEN2 GEN3*
	MXM PCIe Port	*x4x4x4x4 x4x4x8 x8x4x4 x8x8* [*x16*]
	CPU1 - IOU2 PCIe Port	*x4x4x4x4 x4x4x8 x8x4x4* [*x8x8*] *x16*
	RTM PCIe Port	*x4x4x4x4 x4x4x8* [*x8x4x4*] *x8x8 x16*
North Bridge, IOH Configuration Intel(R) VT for Directed I/O Configuration	Intel(R) VT-d	*Enabled* [*Disabled*]
	Coherency Support	*Enabled* [*Disabled*]
	ATS Support	[*Enabled*] *Disabled*
North Bridge, QPI Link	Current QPI Link Speed	[Dynamic update]
	Current QPI Link Freq	[Dynamic update]
	Isoc	[*Enabled*] *Disabled*
	QPI Link Speed Mode	*Slow* [*Fast*]
	QPI Link Frequency Select	[*Auto*] *6.4 GT/s 7.2 GT/s 8.0 GT/s*
	QPI Link0s	*Enabled* [*Disabled*]
	QPI Link0p	*Enabled* [*Disabled*]
	QPI Link1	*Enabled* [*Disabled*]
North Bridge, CPU 0/1 DIMM Information	CPU 0/1 Channel 1/2/3 DIMM 0/1	[Dynamic update]
South Bridge PCH Information	Name	[Dynamic update]
	Stepping	[Dynamic update]

Table 13. Radisys default BIOS Chipset menu setup options (continued)

Chipset Menu		
Submenu	Setup Item	Values [Default]
South Bridge SB Chipset Configuration	PCH Compatibility RID	*Enabled* [*Disabled*]
	SMBus Controller	[*Enabled*] *Disabled*
	Periodic SMI	[*Enabled*] *Disabled*
	Wake on Lan from S5	[*Enabled*] *Disabled*
	SLP_S4 Assertion Stretch Enable	[*Enabled*] *Disabled*
	SLP_S4 Assertion Width	*1-2 Seconds* *2-3 Seconds* *3-4 Seconds* [*4-5 Seconds*]
	Deep Sx	[*Disabled*] *Enabled in S5(Battery)* *Enabled in S5* *Enabled in S4 and S5(Battery)* *Enabled in S4 and S5*
	Disable SCU devices	*Enabled* [*Disabled*]
	Audio Configuration	Engineering Mode
	Azalia internal HDMI codec	*Enabled* [*Disabled*]
	High Precision Event Timer Configuration High Precision Timer	[*Enabled*] *Disabled*
South Bridge USB Configuration	All USB Devices	[*Enabled*] *Disabled*
	EHCI Controller 1	[*Enabled*] *Disabled*
	EHCI Controller 2	*Enabled* [*Disabled*]
	USB Port 0 - 4	[*Enabled*] *Disabled*
	USB Port 5 - 13	*Enabled* [*Disabled*]
PCI Express Ports Configuration	DMI Vc1 Control	[*Enabled*] *Disabled*
	DMI Vcp Control	[*Enabled*] *Disabled*
	DMI Vcm Control	[*Enabled*] *Disabled*
South Bridge, ME Subsystem, Intel ME Subsystem Configuration	ME Subsystem (Help)	[*Enabled*] *Disabled*
	ME BIOS Interface Version	[Dynamic update]
	ME Version	[Dynamic update]
	ME FW Status Value :	[Dynamic update]
	ME FW State :	[Dynamic update]
	ME FW Operation State :	[Dynamic update]
	ME FW Error Code :	[Dynamic update]
	ME Ext FW Status Value :	[Dynamic update]
	BIOS Booting Mode :	[Dynamic update]
	Cores Disabled :	[Dynamic update]
	ME FW SKU Information :	[Dynamic update]
Note: The Radisys default setting for each of the above BIOS setup options is indicated with square brackets ([ ]) surrounding the option or the required entry. If multiple choices are available for a menu item, each choice is indicated in *italics*. If there are no required settings for a menu item, that item does not appear in this table.		

Table 14 lists the Radisys default settings for the IPMI menu of the CPM BIOS setup..

Table 14. Radisys default BIOS IPMI menu setup options

IPMI menu		
Submenu	Setup Item	Values [Default]
Top level: IPMI Menu	BMC Self Test Status	[Dynamic update]
	POST Watchdog	[*Enabled*] *Disabled*
	POST Watchdog Timeout	*30 ...* [*150*] *... 600*
	POST Watchdog Policy	*Do Nothing* [*Reset*] *Power Cycle*
	O/S Watchdog Timer	[*Enabled*] *Disabled*
	O/S WDT Timer Timeout	*5 minutes* [*10 minutes*] *15 minutes 20 minutes*
	O/S WDT Timer Policy	*Do Nothing* [*Reset*] *Power Cycle*
IPMI Menu: System Event Log	Enabling/Disabling Options: SEL Components	[*Enabled*] *Disabled*
	Erasing Settings: Erase SEL	[*No*] *Yes, On next reset Yes, On every reset*
	Erasing Settings: When SEL is Full	[*Do Nothing*] *Erase Immediately*
	Custom EFI Logging Options: Log EFI Status Codes	*Disabled* [*Both*] *Error code Progress code*
IPMI Menu: System Information	Product Manufacturer	[Dynamic update]
	Product Name	[Dynamic update]
	Product Part Number	[Dynamic update]
	Product Version	[Dynamic update]
	Product Serial Number	[Dynamic update]
	Board Manufacturer	[Dynamic update]
	Board Product Name	[Dynamic update]
	Board Version	[Dynamic update]
	Board Serial Number	[Dynamic update]
Note: The Radisys default setting for each of the above BIOS setup options is indicated with square brackets ([ ]) surrounding the option or the required entry. If multiple choices are available for a menu item, each choice is indicated in *italics*. If there are no required settings for a menu item, that item does not appear in this table.		

Table 15 lists the Radisys default settings for the remaining (Security, Boot, and Exit menus) of the CPM BIOS setup..

Table 15. Radisys default BIOS Security, Boot, and Exit menu setup options

Security, Boot, and Exit Menus		
Submenu	Setup Item	Values [Default]
Security Page		
Security	Password Description	*Enabled* [*Disabled*]
Boot Page		
Boot Configuration	Setup Prompt Timeout	[*10*]
	Bootup NumLock State	[*On*] *Off*
	Quiet Boot	*Enabled* [*Disabled*]
	MR-Reset	*Enabled* [*Disabled*]
	Persistent Memory Size	[*0*]
	CSM16 Module Verison	[Dynamic update]
	GateA20 Active	[*Upon Request*] *Always*
	Option ROM Messages	[*Force BIOS*] *Keep Current*
	Interrupt 19 Capture	*Enabled* [*Disabled*]
Boot Option Priorities	Boot Option #xxxx	[Dynamic update]
Save & Exit Page		
	Save & Exit options	*Save Changes and Exit* *Discard Changes and Exit* *Save Changes and Reset* *Discard Changes and Reset*
	Save options	*Save Changes* *Discard Changes* *Restore Defaults* *Save as User Defaults* *Restore User Defaults* *Boot Override*
Note: The Radisys default setting for each of the above BIOS setup options is indicated with square brackets ([ ]) surrounding the option or the required entry. If multiple choices are available for a menu item, each choice is indicated in *italics*. If there are no required settings for a menu item, that item does not appear in this table.		

RAS support

The CPM uses Reliability, Availability and Serviceability (RAS) features to support enhanced boot reliability and reduce system downtime. The following features promote RAS support:

- BIOS protection and redundancy
- Memory error handling
- PCIe error handling
- Processor and integrated memory controller error handling
- POST error handling
- Watchdog support
- BIOS crisis recovery

The system BIOS monitors errors and manages pre-boot and boot events to enhance system uptime. These BIOS actions assist with the management activities performed by the IPMI subsystem and system OS to affect overall system RAS.

BIOS protection and redundancy

Prior to OS boot the BIOS checks the primary boot image checksum and notifies the IPMC if there is a problem. If there is a problem with the primary boot image, the IPMC switches to the standby version and resets the system.

After boot and during normal operation, the IPMC Corrupt Flash Watchdog forces a switch to the secondary boot image by the IPMC if a corrupt boot image is detected that could prevent validation or cause a system hang.

During normal operation, the BIOS program maintains an active write protection on the primary boot image stored in Flash. A jumper is also available at the Customer header to add a physical write protection for the BIOS image.

Memory error handling

Memory error detection and much of the memory error handling is performed by the integrated memory controllers (iMCs) in the CPUs, but the BIOS supports only a subset of the memory RAS features detected by the iMC.

At POST, the system BIOS uses SPD data on each memory module to allow the iMC to find its optimal operating point, or “train” the module and set the optimal operating point for that module. If a module cannot be “trained” or there are any errors detected during the memory training process, the error is reported to the IPMC.

At runtime, the CPU triggers a System Management Interrupt (SMI) when memory errors reach a preset threshold. If the runtime error logging is enabled. then SMI determines the cause, clears the error status, and reports the memory error to IPMC. Memory errors can be either correctable or uncorrectable. If the count of correctable memory errors goes above the BIOS "Max Mem Err Events" value, the SMI handler reports that the correctable error limit has been exceeded and disables further correctable error reporting (thus preventing performance degradation). Uncorrectable memory errors are also reported to IPMC, but error handling is determined by BIOS and OS settings.

PCIe error handling

The BIOS uses both legacy PCI error signaling (PERR/SERR) and PCI Express Advanced Error Reporting (AER). The AER mapping reports the error severity (correctable, uncorrectable/non-fatal, or uncorrectable/fatal) in addition to reporting the error.

If the BIOS has been set up to enable PCI error logging support, the BIOS enumerates all PCI devices detected on the system at POST time, and enables the error reporting – PERR/SERR for legacy devices and AER reporting if the device supports it. The BIOS applies an error mask to all AER-supported devices when errors are reported, and may trigger critical error action for detected AER errors of the proper severity.

As with memory errors, at runtime PCI errors are signaled to SMI. The PCI device causing the error is next determined. The SMI routine then clears the error status and reports a platform event to IPMC. The SMI handler may then trigger critical error action depending on BIOS setup options.

Processor and integrated controller error handling

The CPUs as well as the integrated QuickPath Interconnect (QPI) and Integrated I/O (IIO) controllers implement various types of error detection, correction, containment, and reporting features.

Processor core and uncore error reporting is performed via Machine Check Architecture (MCA). At startup or after a power-good reset, BIOS initializes the machine check registers, clears the status registers by writing zeros into the registers, and writes all ones into the control registers to enable all MCA features. If the system is not coming up from a power-good reset, it retains any error information by preserving the content of machine check status registers.

The QPI protocol uses a CRC mechanism to ensure the data integrity of a serial stream. Unless a “corrupt data containment” mechanism is enabled, the processor generates a QPI error signal on error detection, which in turn generates an SMI for the BIOS to report a platform event.

The IIO module uses an AER mechanism, similar to PCI error handling, to trigger different system error severity responses depending on the type of detected error.

POST error handling

The Power On Self Test (POST) carried out by BIOS after startup examines the functionality of the modules present on the system. It reports any errors to IPMC in the form of platform event messages. The BIOS continues the boot process as long as no errors are detected that might be essential to proper BIOS operation. Errors that might affect BIOS or system operation can cause the BIOS to halt the boot process.

Due to the CPM's design complexity, the initialize time of discovered sub-FRUs can vary significantly from product to product. The BIOS cannot predict sub-FRU initialization time, and some boot devices could be missed if allowance is not made for this variable initialization time.

A BIOS setup option allows user specification of a sub-FRU initialization time so the BIOS waits a specified amount of time before it proceeds with the boot device discovery. Optimization routines shorten the wait time if all the FRUs are either not installed, inactive, or become active before the specified initialization time expires. If communication with the IPMC fails, the BIOS unconditionally waits for the time configured. If any sub-FRU is unable to reach a required FRU state within the time limit, the BIOS reports a system event to the IPMC.

A progressive boot feature causes the BIOS to re-attempt booting the boot devices even if it fails. The "round robin progressive boot" causes the BIOS to attempt booting from the next device in the device list until all boot order entries are tried. The process repeats indefinitely until a boot attempt succeeds, or the system is reset.

Watchdog support

In addition to the RAS features supporting CPM boot, the following watchdog timers support the CPM in the pre-boot and OS runtime environments:

- Corrupt Flash Detection (CFD) watchdog timer
- IPMI Baseboard Management Controller (BMC) watchdog timer

The Corrupt Flash Detection (CFD) watchdog timer is a software-based watchdog implemented in the IPMC to recover the system at boot when the primary BIOS flash is either blank or corrupted. The IPMC starts the CFD watchdog timer at payload reset, and it will force a switch to the secondary boot Flash if it is not stopped within a specified time period.

The Baseboard Management Controller (BMC) watchdog timer is a programmable watchdog timer controlled by the IPMC. The BMC watchdog timer triggers a configurable action (the default action is reset) if some fault condition in the system prevents a stop/strobe of the BMC watchdog. The BMC watchdog timer implementation is based on the IPMI specification and can be configured or disabled by standard IPMI v1.5 commands. Its programmable range is from10 ms to 6,553,600 ms (6553.5 sec) in100 ms (0.1 sec) intervals. By default, BIOS enables the BMC watchdog timer. The IPMC by default disables the BMC watchdog timer after a system reset.

BIOS recovery

Refer to the *Firmware and Software Update Instructions* for the full BIOS image upload procedure.

If the CPM BIOS fails boot due to Flash corruption of both the primary and secondary boot Flash images, the user can recover the Flash BIOS image using a BIOS crisis recovery procedure. When the “BIOS Force Recovery” jumper (pins 5-6) is installed in the customer header (P2), the BIOS images can be reloaded. Refer to *Onboard headers* on page 114 for the full pinout of the CPM customer header.

Once the recovery mode is entered, the system BIOS tries to find and load a BIOS image from either the front panel USB port or the front panel serial port. Once the BIOS image is loaded successfully, the system BIOS continues the subsequent boot phases from the loaded BIOS image until the BIOS image in the flash device is re-programmed. The main and NVRAM BIOS blocks are updated, but not the boot block. Contact Radisys Technical Support for assistance or if the entire BIOS image (including the boot block) needs to be reloaded.

IPMC functions

The IPMC controls the hardware management subsystem by enabling payload power and ports, detecting component hardware states, initiating resets, and monitoring managed sensors.

The CPM’s hardware management system complies with the PICMG 3.0 R3.0 base specification, the HPM.1 R1.0 firmware upgrade specification, and the Intelligent Platform Management Interface (IPMI) 1.5 specification, which defines a set of common interfaces for managing the system and for monitoring system health.

Using serial-over-LAN and IPMI-over-LAN communications, the IPMC provides a remote user with access to the CPU serial console through the base interface. For more information, see *Chapter 4, IPMI-Over-LAN,* on page 63 and *Serial-Over-LAN* on page 65.

The CPM's CPU communicates with the IPMC through a keyboard controller style (KCS) interface, which provides access to IPMI functions. This allows the CPU to send messages to the CPM's IPMC or to any other management controller in the shelf. For a list of the IPMI commands and details on the sensors used on the CPM, refer to *Appendix B, IPMI Commands and Managed Sensors,* on page 86.

Software/Firmware Update Support

Software or firmware update instructions are included in each update package. In the case of a downloaded update package, any update instructions are included as a separate document in the package.

When the software/firmware update is provided on an update CD ROM (ISO) image, the update instructions are included as a separate document on the image along with any other documents associated with the update package.

All upgrades can be performed from the CPM's local CPU:

- Through a serial console that is directly connected to the CPM or RTM serial port.
- Through a remote serial console as described in *Serial-Over-LAN* on page 65.
- By a remote login to the CPM over Ethernet. The session is lost when the CPM reboots. The BIOS setup menus cannot be accessed and the bootup messages cannot be viewed.

Upgrades of the IPMC and IPMC EEPROM can alternatively be performed from a remote computer's CPU:

- By specifying the Shelf Manager IP address and the CPM's IPMB address in the upgrade commands.
- By specifying the CPM's Base interface IP address in the upgrade commands. This method is available when access to the IPMC has been configured as described in *IPMI-Over-LAN* on page 63.

Instructions for upgrading all of the components are included with the upgrade image that is available from the Radisys Web site or from Radisys Technical Support. In all cases, a link in the Release Notes points to a separate *Firmware and Software Update Instructions* manual that provides general update instructions.

Contact Radisys Technical Support if there are problems or if you have questions about the update process.

Operating System Support

The following Linux operating systems are supported for the CPM:

- Red Hat Enterprise Linux, 64-bit
- Monta Vista Carrier Grade Edition Linux, 64-bit
- Wind River Platform for Network Equipment, Linux Edition, version 4.0, 64-bit

Instructions for installing the supported operating systems are included in *ATCA-4xxx CPM Installation Instructions*. Refer to *Software Guide for Management Processors and General Purpose Computing Processors* for more detailed information about installing OS packages. The distribution packages for each supported operating system include detailed installation and configuration instructions.

Contact Radisys Technical Support if there are problems with the initial installation of a supported operating system software package. Contact the operating system manufacturer for technical problems with the OS itself.

Chapter 4

Operation and Maintenance

Introduction

This chapter presents the following operation and maintenance topics:

- Hot swap process
- IPMI over LAN
- Serial over LAN
- Firmware and software upgrades.

Hot Swap of the CPM

The CPM is hot swap capable and meets the hot swap requirements defined in the PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification*. The Shelf Manager controls the hot swap process, and the IPMC enables and disables payload power to the CPM when instructed by the Shelf Manager. Refer to *Removing the CPM* on page 71 and/or *Installing the CPM* on page 72 for detailed procedures on performing a hot swap of the CPM.

IPMI-Over-LAN

A remote management application can establish an IPMI-over-LAN session with the IPMC. The IPMC is remotely accessible through the Base Ethernet ports. The CPM implements IPMI-over-LAN using RMCP and RMCP+ as described in the IPMI 2.0 specification. The IPMI-over-LAN session can be used to enable the functionality described in *Serial-Over-LAN* on page 65.

Configuring IPMI-over-LAN access

The CPM must be initially configured to make IPMI-over-LAN access available. The IPMC saves the configuration changes in non-volatile RAM so they are not lost during reboots, hot-swaps, or firmware updates.

Before you begin

1. Gather the following resources:
   - A remote computer with network access to the Shelf Manager in the shelf with the CPM.

     Note: The initial steps can be run directly on the CPM's CPU as an alternative.
   - An *rsys-ipmitool* utility (available on the software installation CD).

2. Be prepared to fill in values for these variables:

<ShMgr_IP>	The IP address of the Shelf Manager.
<IPMB>	The IPMB address of the CPM in the shelf.
<channel>	The IPMI channel number representing the CPM Base interface channel. Channel 5 is base interface channel 2, and channel 6 is base interface channel 1.
<IP>	The static IP address to assign to each CPM Base interface channel.
<protocol>	The protocol to use (`lan` for RMCP or `lanplus` for RMCP+). The configuration steps are done only once and apply to both protocols.

IPMI-over-LAN basic configuration steps

From the Linux prompt:

1. Set the IP address for a Base interface channel:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **lan set** *<channel>* **ipaddr** *<IP>*

   The `-I` option specifies the IPMI interface to use (`lan`), and the `-A` option specifies an authentication type to use during session activation (**none**). The other command options are defined in Step 2 on the previous page.

   Tip: The previous command assumes *rsys-ipmitool* is executed from a remote Linux computer connected to the Shelf Manager over the IP network. To run the commands directly on the CPM's CPU, omit the `-I, -H, -A, and -t` options. This shortens the above command to:

   `rsys-ipmitool lan set <channel> ipaddr <IP>`

2. Repeat Step 1 to set the IP addresses for any other channels.
3. View the current settings for each channel:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **lan print** *<channel>*

IPMI-over-LAN additional configuration steps

If IPMI-over-LAN does not work after performing the basic steps:

1. Set the user privileges for both channels:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **user priv 1 4 2**

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **user priv 2 4 2**

2. Set the channel and administrator access for a channel:

   rsys-ipmitool -I lan -H *<ShMgr_IP>* -A none -t *<IPMB>* raw 06 0x40 *<channel>* 0x42 0x44

   rsys-ipmitool -I lan -H *<ShMgr_IP>* -A none -t *<IPMB>* raw 06 0x40 *<channel>* 0x82 0x84

   rsys-ipmitool -I lan -H *<ShMgr_IP>* **-A none -t** *<IPMB>* **channel getaccess** <channel> **01**

```
rsys-ipmitool -I lan -H <ShMgr_IP> -A none -t <IPMB> channel setaccess <channel>
01 ipmi=on link=on privilege=4
```

3. Repeat Step 2 to set access to the other channel.

IPMI-over-LAN troubleshooting steps

1. View the current settings for a channel:

   ```
   rsys-ipmitool -I <protocol> -H <ShMgr_IP> -A none -t <IPMB> lan print <channel>
   ```

2. Verify that the IP address is correct.
3. Verify that a non-zero MAC address is set.

   A MAC address of 00:00:00:00:00:00 indicates the Ethernet controller is not responding to queries. This can occur if the Ethernet controller does not have the correct EEPROM file. Upgrade the Base EEPROM image and the front/rear Ethernet EEPROM image using the image files and instructions from the Radisys software distribution.

4. Repeat steps 1–3 to check the settings for the other channel.

Serial-Over-LAN

Serial-over-LAN (SOL) is the specification of packet formats and protocols for transmitting serial data over a LAN using IPMI-over-LAN packets. SOL operation is conceptually straightforward. A remote management application can establish an IPMI-over-LAN session with the IPMC. Once the session is established, the remote console can request SOL session activation.

In SOL mode, any outgoing characters from the PCH are assembled into packets by the IPMC and sent to the remote console over one of the Base LAN interfaces. Conversely, inbound LAN packets carrying characters for the system serial controller have their character data extracted by the IPMC and delivered to the baseboard serial controller.

The SOL character data is contained in SOL messages carried in UDP datagrams. The packet format is “IPMI v2.0 RMCP+” with the payload type set to “SOL”.

Note: The CPM supports one SOL session at a time. The session must be closed before another session can be opened (through the other Base interface channel).

Establishing a SOL session

Prerequisite: This procedure assumes that the required setup for IPMI-over-LAN has been done once for this CPM. For details, see *Configuring IPMI-over-LAN access* on page 63.

One-time SOL configuration steps

The following two steps configure the CPM for SOL:

1. In the CPM BIOS Setup, change the active serial port to COM1, as follows:
   `Advanced Settings > Serial Port 1 Configuration > Serial port: Enabled`
2. Set the Linux console parameters to COM1 (ttyS1) to support SOL.

To configure retry settings from a remote computer:

Important: For these one-time steps, use the Radisys-supplied *rsys-ipmitool* utility.

3. Configure the retries to keep SOL sessions open for a Base interface IP address.
   `rsys-ipmitool -I` *`<protocol>`* **`-H`** *`<IP>`* **`-A none -C 0 sol set retry-interval 0xF0`**
   `rsys-ipmitool -I` *`<protocol>`* **`-H`** *`<IP>`* **`-A none -C 0 sol set retry-count 7`**

   For an explanation of *`<protocol>`* and *`<IP>`*, see *Before you begin* on page 63.
4. Repeat Step to configure retries for the other Base interface IP address.
5. View the retry settings for a Base interface IP address.
   `rsys-ipmitool -I` *`<protocol>`* **`-H`** *`<IP>`* **`-A none -C 0 sol info`**

   The retry count should be 7, and the retry interval should be 2400 ms.
6. Repeat Step 5 to verify access to the remaining interface IP addresses.
7. The SOL payload is disabled by default. Enter the following command to enable it:
   `rsys-ipmitool -I` `lanplus` **`-H`** *`<IP>`* **`-A none -C 0 sol payload enable`**

Note: For proper SOL operation during BIOS POST and at OS runtime, the BIOS console, OS console, and SOL baud rates must all agree. The default SOL parameters include a 38400 baud rate instead of the default BIOS console redirection baud rate of 115200. The 38400 baud rate might be better at avoiding character drops during a SOL session.

8. Both the volatile and non-volatile bit rates must be set to the same value. Enter the following commands to set the baud rate to 115200:
   `rsys-ipmitool -I lanplus -H <IP> -A none -C 0 sol set non-volatile-bit-rate 115.2`
   `rsys-ipmitool -I lanplus -H <IP> -A none -C 0 sol set volatile-bit-rate 115.2`

SOL session open steps

To open a SOL session from a remote computer:

1. Activate the SOL console window:

   rsys-ipmitool -I *<protocol>* **-H** *<IP>* **-A none -C 0 sol activate**

   The SOL session is established.

2. Perform an action (such as pressing Enter) from the SOL console window.

   The SOL console window should respond.

SOL session close step

Note: Only one SOL session can be open at a time to a single CPM.

To terminate a SOL session directly from the active SOL window, enter these characters:

~.

To terminate a SOL session from another window, enter:

rsys-ipmitool -I *<protocol>* **-H** *<IP>* **-A none -C 0 sol deactivate**

Firmware and software upgrade

The processes of updating onboard CPM firmware and associated software are covered in separate documents. Overall upgrade instructions for onboard firmware and software using *rsys_update* tools are covered in detail in the *ATCA Firmware and Software Update Instructions* document. If using Firmware Upgrade Management Instruments (FUMI) tools to perform the upgrade, refer to the *ATCA Firmware and Software Update Instructions Using the Radisys Software Management Framework* document for update instructions. If you have special update requirements, contact Radisys Technical Support for assistance.

Overview of firmware updates

Table 16 summarizes the CPM's programmable devices and the content that can be updated.

Table 16. Programmable devices and upgradeable content

Programmable device	Upgradeable content	Copies to update	Run update commands on
SPI flash	BIOS	2	CPM's CPU
SPI flash	ME	1	CPM's CPU
IPMC	IPMI code	2	CPM's CPU or remote CPU
IPMC EEPROM	FRU records	1	CPM's CPU or remote CPU
SAS EEPROM	LSI SAS EEPROM	1	CPM's CPU
Base NIC	EEPROM image	1	CPM's CPU
Fabric NIC	Firmware	1	CPM's CPU

All updates can be performed from the CPM's local CPU:

- Through a serial console that is directly connected to the CPM or RTM serial port.
- Through a remote serial console as described in *Chapter 4, Serial-Over-LAN,* on page 65.
- By a remote login to the CPM over Ethernet. The session is lost when the CPM reboots. The BIOS setup menus cannot be accessed and the bootup messages cannot be viewed.

Updates of the IPMC and IPMC EEPROM can alternatively be performed from a remote computer's CPU:

- By specifying the Shelf Manager IP address and the CPM's IPMB address in the update commands.
- By specifying the CPM's Base interface IP address in the update commands. This method is available when access to the IPMC has been configured as described in *Chapter 4, IPMI-Over-LAN,* on page 63.

Instructions for upgrading all necessary components are included with the update image, which is available from Radisys Technical Support.

Chapter 5

Troubleshooting and Repair

Introduction

The procedures presented or referenced in this chapter detail removal and replacement of CPM Field Replaceable Units (FRUs) and provide troubleshooting procedures that can be used to discover FRU's that need to be repaired or replaced. The following CPM-related items can be installed or replaced:

- The CPM itself. For installation instructions, see the *ATCA-4xxx Compute Processing Module Installation Guide*. For replacement instructions, see *CPM replacement procedures* on page 71.
- The DIMMs. For placement information and installation and removal instructions, see *Memory module replacement procedures* on page 73.
- An MXM module. For installation or removal procedures, see *MXM module installation/replacement procedures* on page 75.
- The eUSB modules. For installation or removal procedures, see *eUSB module installation/replacement procedures* on page 76.
- A compatible RTM. For installation and removal instructions, see the *Rear Transition Module Installation Guide*.

Refer to *Troubleshooting Topics* on page 77 for troubleshooting procedures to use on the CPM.

Field Replaceable Units (FRUs)

FRU information is stored in non-volatile memory and is used by the IPMC to locate and communicate with the available FRUs. The CPM stores its FRU information in compliance with these specifications:

- *IPMI Platform Management FRU Information Storage Definition*, v1.0, Revision 1.1
- PICMG 3.0 Revision 2.0 *AdvancedTCA Base Specification*

The *rsys-ipmitool* utility can retrieve all FRU information, including backplane E-Keying and on-board E-Keying information.

FRU information areas used

The CPM provides this FRU information:

- Common header
- Internal use area
- Board information area
- Product information area
- Multirecord area

Some of the multirecord area records used are:

- Carrier information record
- Carrier activation and current management record
- Board point-to-point connectivity record
- Carrier point-to-point connectivity record
- Carrier clock point-to-point connectivity record

CPM and FRU device IDs

The CPM IPMC contains unique identification information. Table 17 describes those identifiers.

Table 17. CPM ID information

Field	Value
Device Name	ATCA-46xx
Device ID	012h
Firmware Version	<Current Firmware Version in format XX.YY>
IPMI Version	1.5
IPM Support	029h
Product ID	01715h
Manufacturing ID	0010F1h
CPM main board FRU ID	0

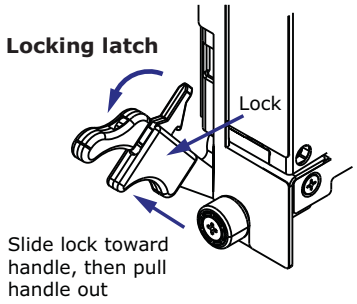
CPM replacement procedures

Removing the CPM

The following steps explain the hot-swap procedure for replacing the CPM:

1. Read *Electrostatic discharge* on page 10 and make sure you are adequately grounded before handling any of the modules.
2. Before replacing the CPM, disconnect all cables from the front panel.
3. Loosen the two thumbscrews securing the CPM.
4. Release the module locking ejector latch that contains the hot-swap switch. This will be either the right or the bottom ejector latch, depending on whether the module is oriented vertically or horizontally.

   To release the locking ejector latch, first disengage the latch lock by sliding the lock toward the handle to release the catch from the shelf latch rail, then pull the handle out. Refer to the illustration.

   Do not release the other latch at this time.

   When the handle or ejector latch is opened, a signal is sent to the IPMC which causes the blue hot-swap LED to begin blinking.

   WARNING!

   - **Never force open a locking ejector latch. The locking mechanism must be disengaged to release the latch or damage to the latch could occur.**
   - **Do not remove a CPM before its hot-swap LED turns solid blue. Removing it prematurely can cause unpredictable results in other parts of the system.**
5. When it is safe to remove the module, the hot-swap LED stops blinking and remains on.

   WARNING! Be careful not to touch any heatsinks when removing the CPM because they might be hot to the touch. If possible, wait 3 to 5 minutes after the hot-swap LED turns solid blue to give the air flow in the system time to cool the board.

   To remove the CPM, release the other locking ejector latch (the non-hot swap latch), using the same release process described in step 4. Simultaneously pull both ejector latches to disengage the module from the backplane and remove it from the chassis.
6. Place the CPM on a flat, static-free surface.
7. ***Important:*** If the removed CPM will not be replaced with another module, install an airflow management filler designed for the slot to maintain proper cooling and airflow through the shelf for the remaining modules.

Removing the CPM board cover

The CPM cooling shroud consists of the main board cover. The entire cover is attached to the board with a number of flat Phillips head screws. Perform the following steps to remove the CPM main board cover:

1. Power down the CPM or activate the hot swap switch so it can safely be uninstalled.
2. Remove the CPM from its slot and set it on an ESD-safe work surface as described in *Removing the CPM* on page 71.
3. Remove the six screws securing the board cover to the board standoffs and set them aside.
4. Remove the board cover and set it aside.

Installing the CPM board cover

Perform the following steps to install the CPM main board cover:

1. Align the board cover so the countersunk screw holes are aligned with the board standoffs.
2. Attach the board cover using six flat-head Phillips screws.

Installing the CPM

The replacement CPM should already be on a static-free surface. Perform the following steps to install the replacement RTM or CPM.

1. Read *Electrostatic discharge* on page 10 and make sure you are adequately grounded before handling any of the modules.
2. Pick up the CPM.
3. Hold the ejector latches in the open position and slide the module all the way into the shelf, making sure it makes a solid connection with the backplane and the EMC gasket forms a tight seal.
4. When the ejector latches reach the latch rail on the shelf, close both ejector latches and tighten the thumbscrews.
5. When a CPM is installed in a shelf with power applied, the blue hot swap LED flashes until the module is active, then turns off.
6. For more information on installing a CPM, see the *ATCA-4xxx Compute Processing Module Installation Guide.*
7. Remove the grounding wrist strap when you are done handling the module.

Memory module replacement procedures

Note: While the ATCA-46xx CPM can operate using a wide range of DIMM memory combinations, at least one DIMM module should be installed in each CPU DIMM bank to ensure there are not boot initialization errors.

Adding or replacing memory modules

Replacing DIMMs consists of removing the CPM from the shelf, removing the main board cover, removing any DIMMs to be replaced, installing the new DIMMs, replacing the main board cover, and re-installing the CPM in the shelf. The following sections detail these procedures.

WARNING! Observe appropriate ESD precautions when performing the procedures in this chapter (see *Electrostatic discharge* on page 10).

Supported DIMM combinations

The CPM normally uses registered DIMMs (RDIMMs) in full sets of twelve identical modules. The supported module kits are as follows:

- A4600-MEM-48GB: This is a set of twelve modules of 4GB DDR3 VLP RDIMMs.
- A4600-MEM-96GB: This is a set of twelve modules of 8GB DDR3 VLP RDIMMs.

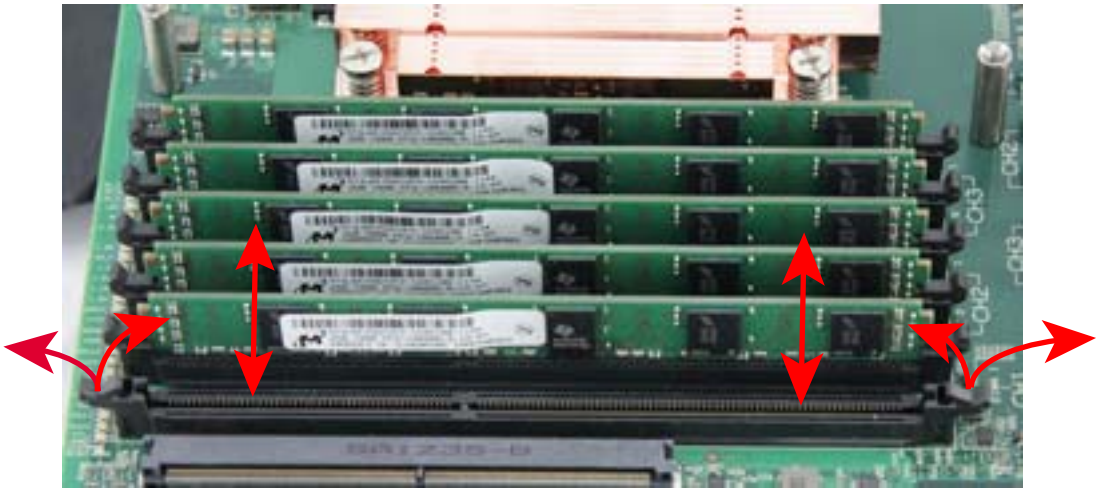
Note: The CPM can support memory module sets of DDR3 VLP RDIMMs in capacities of 1GB, 2GB, 4GB, 8GB, 16GB and 32GB per module as long as maximum memory temperature for the modules is not exceeded.

Removing DIMMs

These instructions assume the CPM has been removed from the shelf and the main board cover has been removed.

1. Determine which DIMMs to remove (see previous discussion under *Supported DIMM combinations*).
2. Press outward on the ejector latches to pop out a DIMM, as indicated for the front DIMM socket in Figure 9.

Figure 9. DIMM insertion/removal



3. Hold the DIMM by the edges and remove it.
4. Remove the other DIMMs in the same manner. To replace the DIMM with a new card, follow the steps under *Installing DIMMs*.
5. Screw the main board cover back into place.
6. Power up the CPM and check the BIOS screens to make sure all memory is detected.

Installing DIMMs

These instructions assume that the CPM has been removed from the shelf and the main board cover has been removed.

1. Open the DIMM ejector latches by pushing them outward, as shown in Figure 9.
2. The DIMMs are keyed so they can be inserted in only one way. Hold the DIMM by the edges, align the slot (keyway) of the DIMM with the tab molded in the base of the socket, and push the card down firmly into the socket. The ejector latches close and click into place when the DIMM is firmly seated.
3. Insert the other DIMMs in the same manner.
4. Screw the main board cover back into place.
5. Power up the CPM and check the BIOS screens to make sure all memory is working.

After the DIMMs are installed, verify that the expected memory is available and the memory is valid as described in the following sections.

Verifying DIMM operation

Verify that the BIOS detects and enables all installed memory. The total detected and enabled memory size is reported in the BIOS setup menu (**`Main > Memory Information`**).

If the total amount of detected memory is less than the total physical DIMM memory that is installed, one of the following conditions might be the cause:

- The DIMM is incorrectly installed
- The DIMM is faulty
- The DIMM installation violates the memory population rules

A DIMM that is not detected or enabled properly can be identified through the BIOS setup menu (`Chipset > CPU Socket 0/1 DIMM Information`).

MXM module installation/replacement procedures

Installing an MXM module

There are two types of MXM module supported for the CPM – an MXM video module or the Radisys DSSD MXM module.

Note: Although any video module complying with the MXM specification will install in the CPM's MXM footprint and connector, the constraints imposed by the ATCA board height requires a custom heatsink solution. Only Radisys-qualified MXM video modules (with the Radisys-designed heat sink solution) can be installed in the CPM. Contact Radisys Technical Support if MXM video is necessary.

Figure 10 shows an MXM module being installed in the CPM.

Figure 10. MXM module insertion/removal

Perform the following steps:

1. Remove the CPM from its slot (see *Removing the CPM* on page 71).
2. Remove the CPM cover (see *Removing the CPM board cover* on page 72).
3. Align the MXM module with the MXM connector near the top front of the CPM.

4. Press the MXM module into the MXM connector until it is fully seated.
5. Align the MXM mounting holes with the board standoffs (nearer the CPM front panel) and secure the module with one (DSSD module) or two (MXM video module) screws.
6. Reinstall the CPM cover (see *Installing the CPM board cover* on page 72).
7. Reinstall the CPM in its slot (see *Installing the CPM* on page 72).

Removing an MXM module

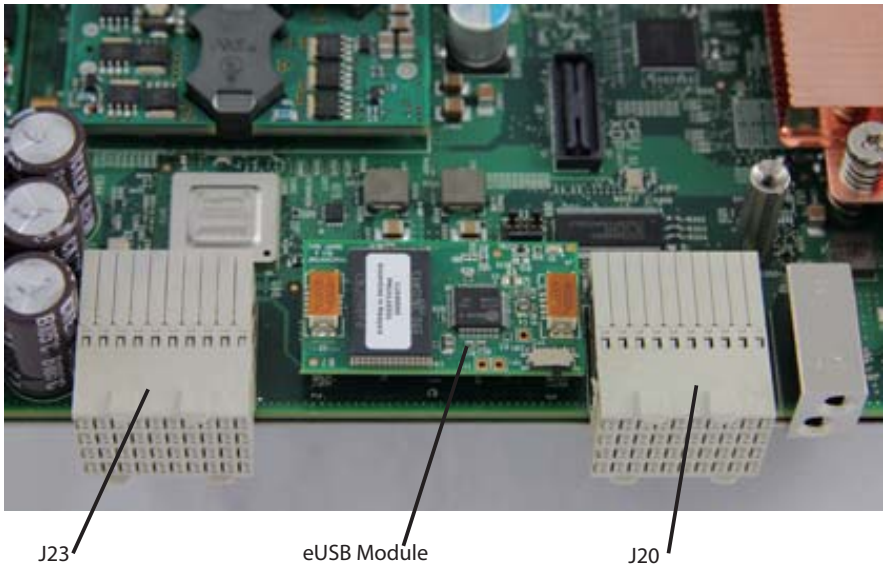
Perform the following steps:

1. Remove the CPM from its slot (see *Removing the CPM* on page 71).
2. Remove the CPM cover (see *Removing the CPM board cover* on page 72).
3. Refer to Figure 10 and locate the MXM module (near the top front of the CPM).
4. Remove the one (DSSD module) or two (MXM video module) screws securing the MXM module to the board standoffs.
5. Disconnect the MXM module from the MXM connector and set it aside.
6. Reinstall the CPM cover (see *Installing the CPM board cover* on page 72).
7. Reinstall the CPM in its slot (see *Installing the CPM* on page 72).

eUSB module installation/replacement procedures

One or two eUSB Flash memory modules can be installed on the ATCA-46xx CPM board. Figure 11shows an eUSB module ready for installation on the board.

Figure 11. eUSB module insertion/removal



Installing an eUSB module

Perform the following steps:

1. Remove the CPM from its slot (see *Removing the CPM* on page 71).
2. Remove the CPM cover (see *Removing the CPM board cover* on page 72).
3. Align the first the eUSB module (between the J20 and J23 connectors at the back of the CPM) over the connectors.
4. Press the first the eUSB module into its connectors until it is fully seated.
5. If there is a second eUSB module, align it over its connectors, then press it in until it is fully seated.
6. Reinstall the CPM cover (see *Installing the CPM board cover* on page 72).
7. Reinstall the CPM in its slot (see *Installing the CPM* on page 72).

Removing an eUSB module

Perform the following steps:

1. Remove the CPM from its slot (see *Removing the CPM* on page 71).
2. Remove the CPM cover (see *Removing the CPM board cover* on page 72).
3. Locate the eUSB module(s) (between the J20 and J23 connectors at the back of the CPM).
4. Disconnect the top eUSB module and set it aside. If there is a bottom eUSB module, disconnect it also and set it aside.
5. Reinstall the CPM cover (see *Installing the CPM board cover* on page 72).
6. Reinstall the CPM in its slot (see *Installing the CPM* on page 72).

Troubleshooting Topics

General troubleshooting tips

When the CPM does not perform as expected, look for symptoms that might point to the cause. Performing the following actions can help diagnose the problem:

- Check the state of the LEDs on the CPM and other modules in the platform, especially the power and out of service LEDs.
- Check temperatures on the CPM. If the Radisys Shelf Manager is used, see the troubleshooting information in the *Shelf Management Software Reference* for details on how to perform these queries.
- Verify the IP address and the subnet mask assignment. See the *Software Guide for Management Processors and General Purpose Computing Processors* for details on verifying these assignments.

Symptoms and recommended actions

Table 18 lists possible troubleshooting scenarios. Look through the listed symptoms to see if any apply to your situation and follow the recommended actions for the applicable symptoms. When an action reveals the cause of the problem, resolve the problem as indicated.

Table 18. Troubleshooting actions based on symptoms

Symptom	Recommendation

The power LED on the CPM is not lit.	• Make sure the CPM is completely inserted and the hot swap latch is engaged.
	• Verify that other modules in the shelf are powered. If not, check the power to the shelf.
	• Inspect the rear connectors for damage. If they show no sign of damage, try the following:
	  • carefully insert the CPM into a different slot
	  • carefully insert a different CPM in the original slot
	WARNING! Do not force the insertion of the CPM. If insertion is not easy, the pins on the backplane connector might be damaged, which could potentially damage the rear connectors on the CPM.
	• Verify the CPM is in the M4 hot swap state (active state). (See the *Shelf Management Software Reference* for more information on hot swap states.)
	• Check to see if the software installed on the CPM is communicating with the platform's Shelf Manager or whether the CPM is waiting for an external Shelf Manager to enable it.

The CPM or another module overheats.	• Verify that a generic front panel is not installed in the shelf. Instead, empty slots must have air management filler panels designed for the shelf's slots installed to properly maintain airflow and emissions. • Check temperatures at the air intake on the overheating module and at the platform's air exhaust. Use the information to determine whether the overheating might be caused by warm facility air, a module failure, or a failed fan module. If the Radisys Shelf Manager is used, see the troubleshooting information in the *Shelf Management Software Reference* for details on how to perform these queries. • Try moving the module to a different slot to see if that resolves the overheating. • Verify there is clearance of at least two inches between the side of the shelf and the side of the rack cabinet. • Check the shelf's air filter for obstructions and dirt.
Sensors generate alarms or events	See the troubleshooting suggestions under *Sensor alarm troubleshooting* on page 79.
The CPM does not work correctly.	Check the Shelf Manager's system event log for significant events related to the CPM. In particular, verify that the CPM worked correctly when it was installed, and look for any events since then that would explain the changes. If the log information does not reveal useful events, remove the CPM and install it in a different slot. If possible, install another CPM of the same kind in the original slot to help determine whether the CPM is defective.
Intermittently, the CPM experiences random data errors.	Verify that the platform's frame-ground connection is properly connected to a high-quality earth-ground connection. Check for electrical noise at the backplane power connections and at the power entry module power inputs. Consider the possibility of a malfunctioning CPM causing electrical noise on backplane connections.

Table 18. Troubleshooting actions based on symptoms (continued)

Symptom	Recommendation
The login prompt does not appear after BIOS has booted.	• Verify the serial cable is plugged into both the CPM and the system with the serial connection. • Verify the CPM is inserted into one of the shelf's node slots. • Verify the terminal emulation application is set to 115200 bps, no parity, 8 data bits, 1 stop bit, with no flow control. • Verify the default Linux port speed has not been changed in the */boot/grub/grub.conf* or */etc/inittab* file.
Message: Operating system not found.	• Make sure an operating system is present on the selected boot media. • Verify the correct device is first in the list in the BIOS boot menu. • Verify that an appropriate network link is available between the CPM and the network boot device.

Sensor alarm troubleshooting

Table 38 on page 96 lists the IPMI managed sensors for the CPM. The table also provides sensor descriptions and threshold values, discrete values, or reported states that might cause the IPMC to generate an alarm or perform some other action. You can use a reported value or state of a managed sensor to troubleshoot problems in the CPM. The managed sensor name, address, and description provide a starting point for isolating a board problem.

Appendix A

Specifications

The Radisys ATCA-46xx CPM complies with or meets the standards and specifications presented in the following sections.

Standards and interfaces

Table 19 lists the standards and interfaces that apply to the CPM.

Table 19. CPM Standards and Interfaces

Standards/Interfaces	Description
Standards	• PICMG 3.0 R3.0.1 AdvancedTCA • PICMG 3.1 R2.0 AdvancedTCA Ethernet option 1/9 • European requirements for hazardous materials, ROHS 6/6
Networking	• Intel® I350 Quad Gigabit Ethernet controller • Four 10/100/1000BASE-T ports (two on front panel and two on Base Interface channels 1-2) • Two SMGII/SerDes ports on Zone 3 connector to the RTM • Dual 40GBASE-KX4 Fabric Interface Channels controlled by Mellanox CX3 dual 40GbE controller
Serial ATA (SATA)	Five Serial ATA II ports from PCH, one onboard, four to RTM
Serial Attached SCSI (SAS)	Three SAS ports from LSISAS1064E to RTM
Video interface	•
USB interface	Two USB 2.0 ports on front panel, two ports available on-board, four ports to RTM
Serial interface	One front panel RJ-45 RS-232 port
Mass and Non-Volatile Storage	• On-board 4GB USB NAND Flash • Four SATA and three SAS ports on RTM
Front Panel I/O	• 1x VGA port (DB-15) • 3x USB 2.0 port (Type-A) • 1x RS-232 port (RJ45) • 2x GbE ports (RJ45) • LEDs: OOS, Media, User, Hot Swap, and Base/Fabric status • Recessed reset button
Rear I/O (to RTM)	• PCI-E x4 from Intel C600 series PCH • 1x COM port • 4x USB 2.0 ports • 4x SATA ports from ICH10R • 3x SAS/SATA ports from LSISAS1064E • 2x SerDes ports

Environmental specifications

Radisys does not provide environmental certification testing because any meaningful emissions agency certification must include the entire system. Thus, the CPM is designed and tested to pass the environmental specifications noted below, but it is not certified.

WARNING! This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

The operating environment must provide sufficient airflow across the CPM to keep it within its temperature specification.

Table 20. Environmental specifications

Characteristic	State	Value
Temperature (ambient)	Operating	+5° C to +40° C 30° C/hr rate of change
	Short term operating[a]	–5°C to +55°C 30° C/hr Rate of Change
	Storage	–40° C to +70° C
Relative humidity	Operating	5% to 85% RH non-condensing
	Short term operating[a]	5% to 90%, RH non-condensing at +30°C but not to exceed 0.024 kg water per kg dry air.
	Storage	5% to 90%, RH non-condensing at +40°C but not to exceed 0.024 kg water per kg dry air.
	Short term storage[a]	5% to 95%, RH non-condensing at +40°C but not to exceed 0.024 kg water per kg dry air.
Altitude	Operating	Up to 1800 meters (5,905 feet), +55°C > 1800 meters up to 4000 meters (13,123 feet), derated linearly to +45°C
Shock (drop)	Unpacked Free fall, corners and edges	0 to < 10 kg = 100 mm drop 10 to < 25 kg = 75 mm drop
	Packaged (Unpalletized) Free fall, corners and edges	0 to < 10 kg = 750 mm drop 10 to < 25 kg = 600 mm drop
	Palletized	300 mm free fall drop
Vibration[b]	Non-operating	0.1g rms, 5 to 100 Hz and back, each axis, 0.1 octave/min sine sweep[b]
	Transportation (packaged)	0.5g, 5 to 50 Hz and back, 0.1 octave/min sine sweep 3.0g, 50 to 500 Hz and back, 0.25 octave/min sine sweep
Seismic	Operating	Per Table 6: Telecommunications Specifications (NEBS)

[a] "Short term" is defined as 96 hours maximum with no more than 15 events or 360 hours within one year.

[b] In each direction, for each of three mutually perpendicular axes

Safety specifications

The safety specifications are measured under laboratory ambient temperature and humidity (approximately 55° C and humidity between 30% and 50%). Testing was performed in partnership with a Nationally Recognized Testing Laboratory (NRTL) accredited to provide the required certifications.

Table 21. Safety specifications

Characteristic	Certification	Standard and test criteria
Product Safety–US	Accessory Listing	UL 60950-1 “Safety for Information Technology Equipment”
Product Safety–Canada	Approval	CSA 22.2 #60950-1-03 “Safety for Information Technology Equipment”
Product Safety–EU	Conformance with the Low Voltage Directive	EN 60950-1 “Safety for Information Technology Equipment”
Product Safety–Other	CB Report	IEC 60950-1 “Safety for Information Technology Equipment”

Mechanical dimensions

Table 22. Mechanical dimensions

Characteristic		Value
PCB board	Dimensions	322.25 mm x 280.0 mm +0, –0.3 mm (12.687” x 11.023” +0.0, –0.012”)
	Board thickness	2.156 mm ±0.2 mm (0.0849” ± 0.008”)
CPM with covers	Thickness	30.48 mm (1.5”)
	Weight	6.6 lbs (3 kg)

Electromagnetic compatibility (EMC)

The ESD, EMC, and Immunity specifications are measured with ambient temperature between 20° C and 30° C and relative humidity between 30% and 50%.

Table 23. Electromagnetic compatibility (EMC)

	Characteristic	State	Standard and criteria
Emissions	Radiated emissions	Operating	FCC Part 15, Class A requirement for chassis/system level, Class A objective for blade (See Note 1) EN 55022: 2006, Class A requirement for chassis/system level, Class A objective for blade (See Note 1)
	Conducted emissions	Operating	FCC Part 15, Class A (See Note 1) EN 55022: 2006, Class A (See Note 1)
Immunity	ESD	Operating	EN 61000-4-2 8 KV direct contact, performance criteria B 15 KV air discharge, performance criteria C
	Radiated	Operating	EN 61000-4-3 10 V/m, 30 MHz–10 GHz, 80% AM Performance criteria A
	Fast transient/burst	Operating	EN 61000-4-4 0.5 kV, 5/50 ns, 5 kHz repetition frequency Performance criteria B
	Surge voltages	Operating	EN 61000-4-5 Data ports: 1 kV, 1.2/50 μs or 8/20 μs DC power port: 0.5 kV, 1.2/50 μs or 8/20 μs Performance criteria B
	Conducted immunity	Operating	EN 61000-4-6 0.15–80 MHz, 3 V, 80% AM Performance criteria A
	Magnetic field immunity	Operating	EN 61000-4-8 50 Hz / 1 A/m Performance criteria A

Note: The requirement for the complete system into which the card is installed is to comply with the requirements for Class A equipment. To achieve this objective the individual board/module/card shall comply with all relevant requirements for Class A equipment when installed in a representative host system. As an objective, to provide confidence that the host system shall comply with Class A requirements when configured with multiple boards, the objective is set for board-level emissions to comply with Class A – 6dB radiated emissions requirements and conducted emissions requirements.

Network Equipment Building Standard (NEBS)

The CPM is designed to meet the NEBS requirements listed in

Table 24. Telecommunication specification (NEBS) requirements

Standard	Description
GR-63-CORE, Issue 3	NEBS Requirements: Physical Protection
GR-1089-CORE, Issue 4	Electromagnetic Compatibility and Electrical Safety
SR-3580	Network Equipment – Building Systems (NEBS) Criteria Levels Level 3, indoor contaminants levels
Note: Verification to be performed at system level by Customer	

Additional compliance

In addition to the standards cited that the ATCA-46xx has been designed to meet, the CPM also complies with the following requirements and standards:

- ETS-300-132 Power supply interface at the input to telecommunications equipment
- EN 300 019-2-1, Storage
- EN 300 019-2-2, T2.3 Transportation
- EN 300 019-2-3, T3.1-T3.5 Earthquake zone
- UL60950-1, 2nd Edition
- AS/NZS CISPR22 C-Tick compliance
- CNS 13438 compliance (Taiwan)
- VCCI Class A compliance (Japan)
- GB 9254 compliance (China)
- GB 4943 compliance (China)
- RRL compliance
- China RoHS in regards to EFUP markings on the blade and packaging

Mean time between failures (MTBF)

The board MTBF is designed to meet or exceed 150,000 hours @ +35C per Telcordia SR332 Issue 2, Method 1, Case 3. The calculation results in Table 25 were generated using the references and assumptions listed. This specification and its associated calculations supersede all other released mean time between failures (MTBF), annual failure rate (AFR), early return index (ERI), and dead-on-arrival (DOA) calculations with earlier dates. The reported failure rates do not represent catastrophic failure.

Table 25. Reliability estimate data

Product	MTBF	AFR	ERI	DOA
ATCA-4616	220,000	4.0%	19,992 PPM	3,320 PPM
ATCA-4618	218,000	4.0%	20,105 PPM	3,351 PPM
ATCA-4648	218,000	4.0%	20,105 PPM	3,351 PPM
Note: Calculations based on the CPM only; does not include DIMMs, on-board modules, or RTM. MTBF - predicted/modeled mean time before failure rate AFR - predicted/modeled annual failure rate at 35°C assuming 100% duty cycle ERI - expected Early Return Index defined as failures in the first 6 months DOA - expected Dead on Arrival rate defined as failures in first 30 days				

Environmental assumptions

- Failure rates are based on a 55° C ambient temperature.
- Applied component stress levels are 50% (voltage, current, and/or power).
- Ground, fixed, controlled environment with an environmental adjustment factor equal to 1.0.

General assumptions

- Calculation Type: MTBF/FIT rate
- Standard: Telcordia Standard SR-332 Issue 2
- Methods: Method I, Case III, Quality Level II
- Component failure rates are constant.
- Board-to-system interconnects are included within estimates.
- Non-electrical components (screws, mechanical latches, labels, covers, etc.) are not included in estimates.

General notes

- Method I, Case I = Based on parts count. Equipment failure is estimated by totaling device failures rates and quantities used.
- Quality Level II = Devices purchased to specifications, qualified devices, vendor lot-to-lot controls for QLs and DPMs.

Where available, direct component supplier predictions or rates have been used.

Appendix B

IPMI Commands and Managed Sensors

IPMI command interfaces

The following interfaces use IPMI command support:

- I^2C bus connections with the following links:
  - I^2C bus 0 - IPMB0-A
  - I^2C bus 1 - IPMB0-B
  - I^2C bus 2 - access to IPMC FPGA, CC FPGA, and RTC circuitry
  - I^2C bus 3- access to voltage monitoring, MXM, and PCIe retimer
  - I^2C bus 4 - SOL access to GbE controller and base/front panel Ethernet
  - I^2C bus 5 - access to PCH (thermal monitoring), IPMB-L, and RTM
- Serial connections using the SCI interface, as follow:
  - SCI1 - link to an external debug board via an onboard debug header
  - SCIF - SOL interface via front panel serial (COM) port
  - SCI3 - provides link to IPMC console while/if SCI1 link connected
- Payload processor link implemented as a KCS port

IPMI commands

Table 26 presents the commands supported by the CPM in different interfaces. These commands are compatible with IPMI v1.5 and PICMG 3.0 R2.0 ECN001.

Table 26. Supported IPMI Commands

IPMI Command name	NetFn Code	Command Code
Get Device ID	App (06h)	01h
Cold Reset	App (06h)	02h
Warm Reset	App (06h)	03h
Get Self Test Results	App (06h)	04h
Set ACPI Power State	App (06h)	06h
Broadcast “Get Device ID”	App (06h)	01h
Reset Watchdog Timer	App (06h)	22h
Set Watchdog Timer	App (06h)	24h
Get Watchdog Timer	App (06h)	25h
Set BMC Global Enables	App (06h)	2Eh
Get BMC Global Enables	App (06h)	2Fh
Clear Message Flags	App (06h)	30h
Get Message Flags	App (06h)	31h
Get Message	App (06h)	33h

Table 26. Supported IPMI Commands (continued)

IPMI Command name	NetFn Code	Command Code
Send Message	App (06h)	34h
Get Channel Authentication Capabilities	App (06h)	38h
Get Session Challenge	App (06h)	39h
Activate Session	App (06h)	3Ah
Set Session Privilege Level	App (06h)	3Bh
Close Session	App (06h)	3Ch
Get Session Info	App (06h)	3Dh
Get AuthCode	App (06h)	3Fh
Set Channel Access	App (06h)	40h
Get Channel Access	App (06h)	41h
Get Channel Info	App (06h)	42h
Set User Access	App (06h)	43h
Get User Access	App (06h)	44h
Set User Name	App (06h)	45h
Get User Name	App (06h)	46h
Set User Password	App (06h)	47h
Activate Payload	App (06h)	48h
Deactivate Payload	App (06h)	49h
Get Channel Payload Support	App (06h)	4Eh
Set Event Receiver	S/E (04h)	00h
Get Event Receiver	S/E (04h)	01h
Platform Event (aka “Event Message”)	S/E (04h)	02h
Get Device SDR Info	S/E (04h)	20h
Get Device SDR	S/E (04h)	21h
Reserve Device SDR Repository	S/E (04h)	22h
Set Sensor Hysteresis	S/E (04h)	24h
Get Sensor Hysteresis	S/E (04h)	25h
Set Sensor Threshold	S/E (04h)	26h
Get Sensor Threshold	S/E (04h)	27h
Set Sensor Event Enable	S/E (04h)	28h
Get Sensor Event Enable	S/E (04h)	29h
Get Sensor Reading	S/E (04h)	2Dh
Get FRU Inventory Area Info	Storage (0Ah)	10h
Read FRU Data	Storage (0Ah)	11h
Write FRU Data	Storage (0Ah)	12h
Get SDR Repository Info	Storage (0Ah)	20h
Reserve SDR Repository	Storage (0Ah)	22h
Get SDR	Storage (0Ah)	23h
Get SEL Info	Storage (0Ah)	40h
Get SEL Entry	Storage (0Ah)	43h

Table 26. Supported IPMI Commands (continued)

IPMI Command name	NetFn Code	Command Code
Add SEL Entry	Storage (0Ah)	44h
Partial Add SEL Entry	Storage (0Ah)	45h
Clear SEL	Storage (0Ah)	47h
Get SEL Time	Storage (0Ah)	48h
Set SEL Time	Storage (0Ah)	49h
Set LAN Configuration Parameters	Transport (0Ch)	01h
Get LAN Configuration Parameters	Transport (0Ch)	02h
Get Address Info	PICMG (2Ch)	01h
Get PICMG Properties	PICMG (2Ch)	00h
FRU Control	PICMG (2Ch)	04h
Get FRU LED Properties	PICMG (2Ch)	05h
Get LED Color Capabilities	PICMG (2Ch)	06h
Set FRU LED State	PICMG (2Ch)	07h
Get FRU LED State	PICMG (2Ch)	08h
Set IPMB State	PICMG (2Ch)	09h
Set FRU Activation Policy	PICMG (2Ch)	0Ah
Get FRU Activation Policy	PICMG (2Ch)	0Bh
Set FRU Activation	PICMG (2Ch)	0Ch
Get Device Locator Record ID	PICMG (2Ch)	0Dh
Set Port State	PICMG (2Ch)	0Eh
Get Port State	PICMG (2Ch)	0Fh
Compute Power Properties	PICMG (2Ch)	10h
Set Power Level	PICMG (2Ch)	11h
Get Power Level	PICMG (2Ch)	12h
Bused Resource	PICMG (2Ch)	17h
Set AMC Port State	PICMG (2Ch)	19h
Get AMC Port State	PICMG (2Ch)	1Ah
Set Clock State	PICMG (2Ch)	2Ch
Get Clock State	PICMG (2Ch)	2Dh
Get Target Upgrade Capabilities	PICMG (2Ch)	2Eh
Get Component Properties	PICMG (2Ch)	2Fh
Abort Firmware Upgrade	PICMG (2Ch)	30h
Initiate Upgrade Action	PICMG (2Ch)	31h
Upload Firmware Block	PICMG (2Ch)	32h
Finish Firmware Upload	PICMG (2Ch)	33h
Get Upgrade Status	PICMG (2Ch)	34h
Activate Firmware	PICMG (2Ch)	35h
Query Self Test Results	PICMG (2Ch)	36h
Query Rollback Status	PICMG (2Ch)	37h
Initiate Manual Rollback	PICMG (2Ch)	38h

Table 26. Supported IPMI Commands (continued)

IPMI Command name	NetFn Code	Command Code
*Restore Factory Defaults	OEM Group (2Eh) OEM 1(30h)	05h
*Disable CFD	OEM Group (2Eh) OEM 1(30h)	E7h
*Set WDT Reset Type	OEM Group (2Eh) OEM 1(30h)	A8h
*Switch Active Boot Flash	OEM Group (2Eh) OEM 1(30h)	A9h
*Get Active Boot Flash	OEM Group (2Eh) OEM 1(30h)	AAh
*Set Control State (for debug only)	OEM Group (2Eh) OEM 1(30h)	20h
*Get Control State(for debug only)	OEM Group (2Eh) OEM 1(30h)	21h
* Refer to *OEM command descriptions* on page 89		

OEM command descriptions

Special commands are available to facilitate CPM-specific functionality. The following sections describe the CPM OEM commands.

Restore Factory Defaults command

This command restores the factory default configuration and threshold parameters for onboard sensors. Table 27 is the command description of the Restore Factory Defaults command.

Table 27. Restore Factory Defaults OEM command

Data Type	Byte	Data Field
Data Field	NetFn	0x30
	Command	0x05
	N/A	
Response Field	1	Completion Code

Set Control State command (for debug only)

This command overrides the current firmware setting of the control pin and should therefore only be used in debug situations and never for production coding. Table 28 is the command description of the Set Control State command.

Table 28. Set Control State OEM command

Data Type	Byte	Data Field
Data Field	1	FRU ID
	2	Control number
	3	Control State 00h = de-assert 01h = assert 02h = pulse de-assert 03h = pulse assert
Response Field	1	Completion Code

Get Control State command (for debug only)

This command returns the current state of a control pin. Table 29 is the command description of the Get Control State command.

Table 29. Get Control State OEM command

Data Type	Byte	Data Field
Data Field	1	FRU ID
	2	Control number
Response Field	1	Completion Code
	2	Control State 00h = de-asserted 01h = asserted

Disable CFD command

This command indicates to the IPMC that the CFD Watchdog Timer needs to be disabled. No data byte is required. Table 30 is the command description of the Disable CFD command.

Table 30. Disable CFD OEM command

Data Type	Byte	Data Field
Data Field	N/A	N/A
Response Field	1	Completion Code

Set WDT Reset Type command

This command allows a BMC Watchdog timeout configured for "Hard Reset" to cause a Warm Reset or a Cold Reset. Table 31 is the command description of the Restore Factory Defaults command.

Table 31. Set WDT Reset Type OEM command

Data Type	Byte	Data Field
Data Field	1	Reset Type Configuration: 1 = Warm Reset, 0 = Cold Reset
Response Field	1	Completion Code

Switch Active Boot Flash command

This command sets the current Boot Flash and can cause a cold reset to the x86 Processor Complex portion of the board if the appropriate bits in the command data are set. The command can also set the primary Boot Flash, which is selected during a power-on reset of the blade. Table 32 is the command description of the Switch Active Boot Flash command.

Table 32. Switch Active Boot Flash OEM command

Data Type	Byte	Data Field
Data Field	1	Bit 7 = Sets the primary boot flash 0b (Do not set) 1b (Set primary flash to Flash selected by Bit 0) Bit 6 = Selects whether or not a reset will occur as a result of calling this command 0b (Causes reset), 1b (Does not cause reset) Bits 5:1 = reserved Bit 0 (Boot Flash) = 0b (Boot Flash 0), 1b (Boot Flash 1)
Response Field	1	Completion Code

When bit 7 is set, the Boot Flash selected in Bit 0 is set as the primary boot flash and the other boot flash becomes the secondary. This setting is persistently stored by the IPMC and the primary boot flash designation is maintained over board power cycles and resets.

Get Active Boot Flash command

This command gets the current Boot Flash and the primary Boot Flash from the H8 IPMI firmware. Table 33 is the command description of the Get Active Boot Flash command.

Table 33. Get Active Boot Flash OEM command

Data Type	Byte	Data Field
Data Field	1	FRU ID
Response Field	1	Completion Code
	2	Currently selected Boot Flash
	3	Primary Boot Flash

RTM Reset Button command

This command instructs the H8 IPMI Firmware to perform a COLD reset. Table 34 is the command description of the Get Active Boot Flash command.

Table 34. RTM Reset Button OEM command

Data Type	Byte	Data Field
Data Field	1	Radisys IANA PEN0: F1h
	2	Radisys IANA PEN0: 10h
	3	Radisys IANA PEN0: 00h
Response Field	1	Completion Code
	2	Radisys IANA PEN0: F1h
	3	Radisys IANA PEN0: 10h
	4	Radisys IANA PEN0: 00h

Set Payload Status command

This command informs the H8 IPMI Firmware the current payload processor status. The IPMI firmware may use the reported information to initiate its internal processes which are dependent on resources controllable by the onboard x86 processor complex.

In the CPM, the boot phases 1 and 4 specified in status byte 1 are used to report the commencement and completion of the onboard x86 processor complex boot-up processes. The remaining boot phases are optionally used to report other milestones in the payload boot-up process.

At boot phase 1, the IPMI firmware initializes all appropriate control signals to get all hardware shared resources of the onboard x86 processor complex. At boot phase 4, the IPMI firmware reconfigures the appropriate control signals to get access to all hardware shared resources and begin the applicable management functions. Table 35 is the command description of the Get Active Boot Flash command.

Table 35. Set Payload Status OEM command

Data Type	Byte	Data Field
Data Field	1	Radisys IANA PEN0: F1h
	2	Radisys IANA PEN0: 10h
	3	Radisys IANA PEN0: 00h
	4	Command Version: hard coded to 0x00
	5	Status Byte 1 Bits 7:4 = Reserved Bit 3 (Boot Phase 4) = 0b (Not Complete) 1b (Complete) Bit 2 (Boot Phase 3) = 0b (Not Complete) 1b (Complete) Bit 1 (Boot Phase 2) = 0b (Not Complete) 1b (Complete) Bit 0 (Boot Phase 1) = 0b (Not Complete) 1b (Complete)
	6	Status Byte 2 Bits 7:0 = Reserved
Response Field	1	Completion Code
	2	Radisys IANA PEN0: F1h
	3	Radisys IANA PEN0: 10h
		Radisys IANA PEN0: 00h

Get Payload Status (for debug only) command

This command returns the H8 IPMI Firmware acknowledgement of the payload processor status. The BIOS/OS may use this command to check if the IPMI firmware has finished the internal processes for the onboard x86 Processor Complex boot phase specified in a (previously sent) Set Payload status command.

In the CPM9, after the IPMI firmware has initialized all appropriate control signals to yield access of all hardware shared resources to the onboard x86 Processor Complex, it shall report the completion of boot phase 1. After having reconfigured the appropriate control signals to regain access of all hardware shared resources and commenced the applicable management functions, it shall report the completion of boot phase 4. Table 36 is the command description of the Get Active Boot Flash command.

Table 36. Get Payload Status OEM command

Data Type	Byte	Data Field
Data Field	1	Radisys IANA PEN0: F1h
	2	Radisys IANA PEN0: 10h
	3	Radisys IANA PEN0: 00h
	4	Command Version: hard coded to 0x00
Response Field	1	Completion Code
	2	Radisys IANA PEN0: F1h
	3	Radisys IANA PEN0: 10h
	4	Radisys IANA PEN0: 00h
	5	Command Version
	6	Status Byte 1 Bits 7:4 = Reserved Bit 3 (Boot Phase 4) = 0b (Not Complete) 1b (Complete) Bit 2 (Boot Phase 3) = 0b (Not Complete) 1b (Complete) Bit 1 (Boot Phase 2) = 0b (Not Complete) 1b (Complete) Bit 0 (Boot Phase 1) = 0b (Not Complete) 1b (Complete)
	7	Status Byte 2 Bits 7:0 = Reserved

Managed sensors

On the CPM, the IPMC sensors monitor voltages, temperatures, control signals, and status events. For functional information, refer to *IPMI controller* on page 33. The sensors are described in Table 38.

Types of sensors

The CPM implements the following types of sensors.

- Discrete — A discrete sensor can have up to 16 bitmapped states, with one state as true.
- Digital — A digital sensor has two possible states, only one of which can be active at any given time. For example, a digital sensor monitoring the power may indicate whether the power is good or not good.
- OEM — An OEM sensor has its states defined by the manufacturer. The reading types of these sensors are sometimes defined as “sensor-specific.”
- Threshold — A threshold sensor has a range of 256 values, which represent measurements on the CPM and its FRUs. Temperature, voltage, current, and fan speed sensors are examples of threshold sensors. Table 37 lists the possible threshold types for the managed sensors.

Table 37. Threshold types

Threshold type	Description
UNR	Upper non-recoverable thresholds generate a critical alarm on the high side.
UC	Upper critical thresholds generate a major alarm on the high side.
UNC	Upper non-critical thresholds generate a minor alarm on the high side.
LNC	Lower non-critical thresholds generate a minor alarm on the low side.
LC	Lower critical thresholds generate a major alarm on the low side.
LNR	Lower non-recoverable thresholds typically generate a critical alarm on the low side.

Note: If the CPM exceeds one of the UNR thresholds, the Shelf Manager generates a critical alarm and shuts down the CPM. See the *Software Guide* for details.

IPMI Sensors

The CPM supports a variety of sensors, each with entries in the Sensor Data Records (SDR). Table 38 lists the IPMI sensors supported by the CPM.

Table 38. ATCA-46xx IPMI Managed Sensors

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
0	ATCA FRU Hot swap	ATCA FRU Hot swap	Sensor-specific	0x00 -0x07	This sensor returns the ATCA M0 through M7 hot swap states for the front blade
1	RTM FRU Hot swap	ATCA FRU Hot swap	Sensor-specific	0x00 -0x07	This sensor returns the ATCA M0 through M7 hot swap states for the RTM
2	Version Change	Version Change (IPMI 2.0)	Sensor-specific	0x00 -0x07	
3	OEM Payload Reset	Other Sensor (0xD4)	Sensor-specific	0x00-0xFF	Used to indicate the cause of payload resets that occur during standard operation of the CPM.
4	OEM ActBootFlash	Other Sensor (0x0B	Sensor-specific	0 or 1	Indicates which boot Flash bank the IPMC has currently selected. If the flash select signal changes state, indicates the reason.
5	BMC Watchdog	Watchdog 2	Sensor-specific	N/A	OffsetWatchdog action 0Timer Expired, status only (no action, no interrupt) 1Payload Cold Reset 2Payload Power Down 3Payload Power Cycle 4-7Reserved 8Pre-Timer interrupt
6	IPMC Watchdog	OEM (0xED for IPMC FPGA WDT)	Digital	N/A	Sensor SDR states that this sensor does not return any analog readings (a Get Sensor Reading command directed at this sensor always returns '0' for a reading); however, an "assert" event is logged to the SEL once the IPMC is reset due to the Watchdog.
7	EventLogDisabled	Event Logging Disabled	Sensor-specific	0x00 - 0x20	Contains hex value from 0 to 100 decimal (00h to 64h) representing the SEL filled (%) at the time the event was generated. 00h is 0% full (SEL is empty), 64h is 100% full, etc.
8	ATCA Phys IPMB	ATCA Physical IPMB-0	Sensor-specific	0x00-0xFF	Bit [7] = IPMB B Override State Bit [6:4] = IPMB B Local Status Bit [3] = IPMB A Override State Bit [2:0] = IPMB A Local Status
9	ATCA Phys IPMB-L	ATCA Physical IPMB-0	Sensor-specific	0x00-0xFF	Bit [7:4] = Reserved Bit [3] = IPMB-L Override State Bit [2:0] = IPMB-L Local Status
10	Ejector Closed	Slot or Connector	Digital	1	0 = Eject latch is open. Fault Status asserted 1 = Eject latch is closed. Identify Status asserted
11	RTM Present	Slot or Connector	Digital	0 or 1	0 = RTM is not present 1 = RTM is present
12	ENET Link 0	Slot or Connector	Digital	0 or 1	0 = E0_LINK* not asserted 1 = E0_LINK* asserted

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
13	ENET Link 1	Slot or Connector	Digital	0 or 1	0 = E1_LINK* not asserted 1 = E1_LINK* asserted
14	ENET Link 2	Slot or Connector	Digital	0 or 1	0 = E2_LINK* not asserted 1 = E2_LINK* asserted
15	ENET Link 3	Slot or Connector	Digital	0 or 1	0 = E3_LINK* not asserted 1 = E3_LINK* asserted
16	ENET Link 4	Slot or Connector	Digital	0 or 1	0 = E4_LINK* not asserted 1 = E4_LINK* asserted
17	ENET Link 5	Slot or Connector	Digital	0 or 1	0 = E5_LINK* not asserted 1 = E5_LINK* asserted
18	-48V Absent A	Power Supply	Digital	0 or 1	0 = Power Supply A. Presence detected 1 = Power Supply A. Failure detected
19	-48V Absent B	Power Supply	Digital	0 or 1	0 = Power Supply B. Presence detected 1 = Power Supply B. Failure detected
20	-48V Fuse Fault	Power Supply	Digital	0 or 1	0 = Both A & B fuses OK and both supplies detected 1 = Either A or B fuse blown or only single supply detected
21	System PwrFail	Power Supply	Digital	0 or 1	0 = Power is good 1 = Power fail detected
22	+12V RTM PwrFail	Power Supply	Digital	0 or 1	0 = De-Asserted 1 = Asserted
23	+3.3V RTM Fail	Power Supply	Digital	0 or 1	0 = De-Asserted 1 = Asserted
24	RTM PwrFault	Power Supply	Digital	0 or 1	0 = RTM PwrFault not asserted 1 = RTM PwrFault asserted
25	RTM PCIe PwrEn	Power Supply	Digital	0 or 1	0 = RTM PCIe PwrEn not asserted 1 = RTM PCIe PwrEn asserted
26	RTM PCIe2 PwrEn	Power Supply	Digital	0 or 1	0 = RTM PCIe2 PwrEn not asserted 1 = RTM PCIe2 PwrEn asserted
27	CPU0 ThermTrip	Processor	Digital	0 or 1	0 = CPU ThermTrip not asserted 1 = CPU ThermTrip asserted
28	CPU1 ThermTrip	Processor	Digital	0 or 1	0 = CPU ThermTrip not asserted 1 = CPU ThermTrip asserted
29	CPU MCERR	Processor	Digital	0 or 1	0 = CPU MCERR not asserted 1 = CPU MCERR asserted
30	CPU0 ProcHot	Processor	Digital	0 or 1	0 = CPU ProHot not asserted 1 = CPU ProHot asserted
31	CPU1 ProcHot	Processor	Digital	0 or 1	0 = CPU ProHot not asserted 1 = CPU ProHot asserted
32	CPU IERR	Processor	Digital	0 or 1	0 = CPU IERR not asserted 1 = CPU IERR asserted

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
33	+12V	Voltage	Threshold	12.00	LNR = 0.00 LC = 10.8 LNC = 11.4 UNC = 12.6 UC = 13.2 UNR = 13.8
34	+5V	Voltage	Threshold	5.00	LNR = 0.00 LC = 4.5 LNC = 4.75 UNC = 5.25 UC = 5.49 UNR = 5.74
35	+5V Standby	Voltage	Threshold	5.00	LNR = 0.00 LC = 4.5 LNC = 4.75 UNC = 5.25 UC = 5.49 UNR = 5.74
36	+3.3V IPMI	Voltage	Threshold	3.30	LNR = 0.00 LC = 2.97 LNC = 3.15 UNC = 3.47 UC = 3.64 UNR = 3.8
37	+3.3V	Voltage	Threshold	3.30	LNR = 0.00 LC = 2.97 LNC = 3.15 UNC = 3.47 UC = 3.64 UNR = 3.8
38	+1.8V	Voltage	Threshold	1.80	LNR = 0.00 LC = 1.62 LNC = 1.71 UNC = 1.89 UC = 1.98 UNR = 2.04
39	+1.8V FR	Voltage	Threshold	1.80	LNR = 0.00 LC = 1.62 LNC = 1.71 UNC = 1.89 UC = 1.98 UNR = 2.04

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
40	+1.5V PCH	Voltage	Threshold	1.50	LNR = 0.00 LC = 1.35 LNC = 1.43 UNC = 1.58 UC = 1.65 UNR = 1.73
41	+1.2V	Voltage	Threshold	1.20	LNR = 0.00 LC = 1.08 LNC = 1.14 UNC = 1.26 UC = 1.32 UNR = 1.38
42	+1.1V	Voltage	Threshold	1.10	LNR = 0.00 LC = 0.99 LNC = 1.05 UNC = 1.17 UC = 1.23 UNR = 1.29
43	+1V	Voltage	Threshold	1.00	LNR = 0.00 LC = 0.90 LNC = 0.95 UNC = 1.05 UC = 1.10 UNR = 1.15
44	VCCP0	Voltage	Threshold	1.04 VID = 0.75 ~1.35	LNR = 0.00 LC = 0.72 LNC = 0.76 UNC = 1.31 UC = 1.38 UNR = 1.44
45	VCCP1	Voltage	Threshold	1.04 VID = 0.75 ~1.35	LNR = 0.00 LC = 0.72 LNC = 0.76 UNC = 1.31 UC = 1.38 UNR = 1.44
46	+VDDQ0	Voltage	Threshold	1.50	LNR = 0.51 LC = 1.4 LNC = 1.46 UNC = 1.56 UC = 1.61 UNR = 1.66

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
47	+VDDQ1	Voltage	Threshold	1.50	LNR = 0.51 LC = 1.4 LNC = 1.46 UNC = 1.56 UC = 1.61 UNR = 1.66
48	+VTT0	Voltage	Threshold	1.05 (SNB)/1.0(IVB)	LNR = 0.50 LC = 0.96 LNC = 1.00 UNC = 1.10 UC = 1.12 UNR = 1.16
49	+VTT1	Voltage	Threshold	1.05 (SNB)/1.0(IVB)	LNR = 0.50 LC = 0.96 LNC = 1.00 UNC = 1.10 UC = 1.12 UNR = 1.16
50	+VTT DDR0	Voltage	Threshold	0.75	LNR = 0.50 LC = 0.68 LNC = 0.71 UNC = 0.79 UC = 0.83 UNR = 0.87
51	+VTT DDR1	Voltage	Threshold	0.75	LNR = 0.50 LC = 0.68 LNC = 0.71 UNC = 0.79 UC = 0.83 UNR = 0.87
52	+2.5V FE	Voltage	Threshold	2.5	LNR = 0.00 LC = 2.34 LNC = 2.37 UNC = 2.63 UC = 2.69 UNR = 2.76
53	+VDD FE	Voltage	Threshold	1.2(CX2)/0.9(CX3)	LNR = 0.00 LC = 1.12 LNC = 1.16 UNC = 1.25 UC = 1.28 UNR = 1.32

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
54	+VCCPLL0	Voltage	Threshold	1.8(SNB)/1.7(IVB)	LNR = 0.00 LC = 1.68 LNC = 1.74 UNC = 1.89 UC = 1.95 UNR = 1.99
55	+VCCPLL1	Voltage	Threshold	1.8(SNB)/1.7(IVB)	LNR = 0.00 LC = 1.68 LNC = 1.74 UNC = 1.89 UC = 1.95 UNR = 1.99
56	+VSA0	Voltage	Threshold	0.85	LNR = 0.00 LC = 0..56 LNC = 0.60 UNC = 1.16 UC = 1.20 UNR = 1.25
57	+VSA1	Voltage	Threshold	0.85	LNR = 0.00 LC = 0..56 LNC = 0.60 UNC = 1.16 UC = 1.20 UNR = 1.25
58	+1.2V Standby	Voltage	Threshold	1.20	LNR = 0.00 LC = 1.08 LNC = 1.14 UNC = 1.26 UC = 1.32 UNR = 1.38
59	+LVDDQ0	Voltage	Threshold	1.35(LV DIMM)	LNR = 0.51 LC = 1.26 LNC = 1.30 UNC = 1.41 UC = 1.45 UNR = 1.49
60	+LVDDQ1	Voltage	Threshold	1.35(LV DIMM)	LNR = 0.51 LC = 1.26 LNC = 1.30 UNC = 1.41 UC = 1.45 UNR = 1.49

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
61	+LVTT DDR0	Voltage	Threshold	0.675 (LVDIMM)	LNR = 0.50 LC = 0.63 LNC = 0.65 UNC = 0.70 UC = 0.73 UNR = 0.75
62	+LVTT DDR1	Voltage	Threshold	0.675 (LVDIMM)	LNR = 0.50 LC = 0.63 LNC = 0.65 UNC = 0.70 UC = 0.73 UNR = 0.75
63	Inlet Temp 1	Temperature	Threshold	25	LNR = -10 LC = - 5 LNC = 0 UNC = 80 UC = 90 UNR = 100
64	Inlet Temp 2	Temperature	Threshold	25	LNR = -10 LC = - 5 LNC = 0 UNC = 80 UC = 90 UNR = 100
65	CPU0 DIMM Temp	Temperature	Threshold	25	LNR = N/A LC = N/A LNC = N/A UNC = 72 UC = 80 UNR = 95
66	CPU1 DIMM Temp	Temperature	Threshold	25	LNR = N/A LC = N/A LNC = N/A UNC = 72 UC = 80 UNR = 95
67	PCH Die Temp	Temperature	Threshold	25	LNR = N/A LC = N/A LNC = N/A UNC = 111 UC = 116 UNR = 121

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
68	CPU0 Core DTS	Temperature	Threshold	25	LNR = N/A LC = N/A LNC = N/A UNC = -20 UC = -13 UNR = -1
69	CPU1 Core DTS	Temperature	Threshold	25	LNR = N/A LC = N/A LNC = N/A UNC = -20 UC = -13 UNR = -1
Event-only Sensors					
90	Memory	Memory	Sensor-specific	N/A	Offset Description 00h = Correctable ECC / other correctable memory error 01h = Uncorrectable ECC / other correctable memory error 04h = Memory Device Disabled 05h = Correctable ECC / other correctable memory error logging limit reached 07h = Configuration error Event Data 2 (for both event offsets 4h, 7h): OEM - DIMM location [7:6] - Reserved [5:3] - Channel 00 - Channel 'A' on silkscreen 01 - Channel 'B' on silkscreen 10 - Channel 'C' on silkscreen 11 - Unspecified [2:0] - DIMM 00 ~ 10 - According to the label on silkscreen 11 - Unspecified Event Data 3 (for both event offsets 0h, 1h): [7:6] - Reserved [5:4] - Channel number [3:0] - DIMM number Event Data 3 (for both event offsets 4h, 7h): OEM data
91	Critical Interrupt	Critical Interrupt	Sensor-specific	N/A	04h - PCI PERR 05h - PCI SERR Event Data 2 (for both event offsets 4h, 5h): PCI bus number for failed device Event Data 3 (for both event offsets 4h, 5h): [7:3] - PCI device number for failed device [2:0] - PCI function number for failed device

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
92	Processor	Processor	Sensor-specific	N/A	Offset Description 03h = FRB2/ Hang in POST failure (used hang is believed to be due or related to a processor failure. Use System Firmware Progress sensor for other BIOS hangs.)
93	System Firmware Progress	System Firmware Progress	Sensor-specific	N/A	Offset Description 00h = System Firmware Error (POST error) 01h = System Firmware Hang Event Data 2 (for both 00h and 01h): 00h - Unspecified. 01h - No system memory is physically installed in the system. 02h - No usable system memory, all installed memory has experienced an unrecoverable failure. 03h - Unrecoverable hard-disk/ATAPI/IDE device failure. 04h - Unrecoverable system-board failure. 05h - Unrecoverable diskette subsystem failure. 06h - Unrecoverable hard-disk controller failure. 07h - Unrecoverable PS/2 or USB keyboard failure. 08h - Removable boot media not found 09h - Unrecoverable video controller failure 0Ah - No video device detected 0Bh - Firmware (BIOS) ROM corruption detected 0Ch - CPU voltage mismatch (processors that share same supply have mismatched voltage requirements) 0Dh - CPU speed matching failure

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
93 (cont.)	System Firmware Progress (cont.)				02h = System Firmware Progress Event Data 2: 00h - Unspecified. 01h - Memory initialization. 02h - Hard-disk initialization 03h - Secondary processor(s) initialization 04h - User authentication 05h - User-initiated system setup 06h - USB resource configuration 07h - PCI resource configuration 08h - Option ROM initialization 09h - Video initialization 0Ah - Cache initialization 0Bh - SM Bus initialization 0Ch - Keyboard controller initialization 0Dh - Embedded controller/management controller initialization 0Eh - Docking station attachment 0Fh - Enabling docking station 10h - Docking station ejection 11h - Disabling docking station 12h - Calling operating system wake-up vector 13h - Starting operating system boot process, e.g. calling INT 19h 14h - Baseboard or motherboard initialization 15h - reserved 16h - Floppy initialization 17h - Keyboard test 18h - Pointing device test 19h - Primary processor initialization

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
94	Boot Error	Boot Error	Sensor-specific	N/A	Offset Description 00h = Boot Record Corruption eventData1: 0xA0 - Boot record corruption eventData2: 0x00 - Currently executing Application image does not match non-volatile storage designation eventData3: 0x00 - Currently executing Application image does not match non-volatile storage designation (i.e., running != active) 01h = Boot Failure (IPMC Boot Error) eventData1: 0xA1 - Boot failure error eventData2: 0x00 - Currently executing Application image does not match non-volatile storage designation eventData3: Bits 7:4 == Currently executing Application image number 0x1 - Bank 1 0x2 - Bank 2 Bits 3:0 == Image number specified in non-volatile boot record (active) 0x1 - Bank 1 0x2 - Bank 2 02h = Application Image Corruption (IPMI-FW Application Image Corruption) eventData1: 0xA2 - Application Image Corrupt eventData2: Currently executing Application Image# 0x11 - Bank 1 0x22 - Bank 2 eventData3: Corrupted Application image# 0x11 - Bank 1 0x22 - Bank 2
95	System Event	System Event	Sensor-specific	N/A	Offset Description 01h = OEM System Boot Event 05h = Timestamp Clock Synch
96	OEM HPM Event	OEM (0xEF)	Sensor-specific	N/A	Offset Description 00h = No bootable media)
97	OEM CFD Watchdog	Watchdog 2	Sensor-specific	N/A	Offset Description 03h = Power Cycle
98	Arbitration	OEM SHMC HA State	Sensor-specific	N/A	Offset Description 00h = IPMC Redundancy State (Only applicable if CPM is in IPMB Addr 0x82 and acts as shelf manager) eventData1: 0 eventData2: Current State (10 = active) eventData3: Previous State (03 = standby)

Table 38. ATCA-46xx IPMI Managed Sensors (continued)

Sensor #	Name	Type	Reading Type	Normal Reading	Notes
99	Failover	OEM Failover	Sensor-specific	N/A	Offset Description 00h = OEM Failover (Only applicable if redundancy is available.) eventData1: 0 eventData2: 0 & eventData3: 4' Failover Start eventData2: 1 & eventData3: FF' Failover Complete
100	HPI Event	OEM HPI	OEM	N/A	Offset Description 01h = OEM HPI (Only applicable if Radisys Shelf Manager application is installed.) eventData1: 1 eventData2: 3:0 = channel 7:4 = LUN eventData3: 0
120-254	Open for statically added sensors from MXM and dynamically added sensors from RTM.				

Pinouts and Mapping

The ATCA-46xx CPM pinout listings apply to front panel connectors and the Zone 1 and 2 backplane connectors. The onboard header pinouts apply to user-accessible areas of the CPM board.

Front panel connectors

The following sections describe the pinouts for the front panel connectors.

COM serial connector

Table 39 lists the pinout for the front panel COM serial connector.

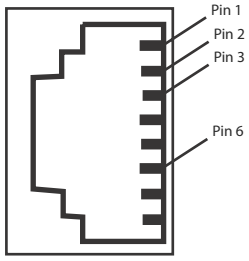


Table 39. COM Serial Connector (J6)

Pin#	Signal	Function
1	RTS	Request to Send
2	DTR	Data Terminal Ready
3	TXD	Transmit Data
4	GND	Ground
5	GND	Ground
6	RXD	Receive Data
7	DSR	Data Set Ready
8	CTS	Clear to Send

Dual USB connectors

Table 40 lists the pinout for each of the front panel dual USB connectors. Note that several unlabeled connection points (near pins 1 and 4) on each connector are connection points between the plug and connector shields.

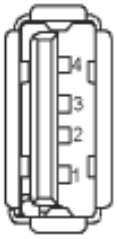


Table 40. Dual USB Connectors (J10)

Pin#	Signal
1	Vcc
2	Data-
3	Data+
4	GND

Dual Ethernet connectors

Table 41 lists the pinout for each of the front panel RJ45 Ethernet GbE connectors. Note that power, ground, and the LED control signals are fed from the PCB and are not accessible at the connector pins. Refer to Table 1 on page 18 for detailed information on the connector LEDs.

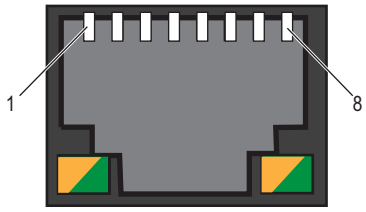


Table 41. Dual Ethernet GbE Connectors (J8)

Pin#	Signal
1	Channel 0 Data +
2	Channel 0 Data -
3	Channel 1 Data +
4	Channel 2Data +
5	Channel 2 Data -
6	Channel 1 Data -
7	Channel 3Data +
8	Channel 3Data -

Mini-DisplayPort connector

Table 42 lists the pinout for the front panel Mini-DisplayPort connector.

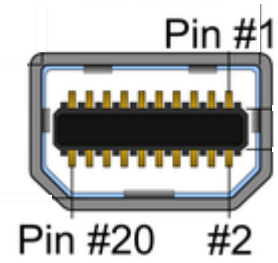


Table 42. Mini-DisplayPort connector (J5)

Pin#	Signal
1	GND
2	Hot Plug Detect
3	ML_Lane 0 (p)
4	CONFIG1
5	ML_Lane 0 (n)
6	CONFIG2
7	GND
8	GND
9	ML_Lane 1 (p)
10	ML_Lane 3 (p)
11	ML_Lane 1 (n)
12	ML_Lane 3 (n)
13	GND
14	GND
15	ML_Lane 2 (p)
16	AUX_CH (p)
17	ML_Lane 2 (n)
18	AUX_CH (n)
19	GND
20	DP_PWR

Backplane interfaces

Backplane connectivity summary

This section describes the backplane interface connectivity. Table 43 lists the backplane connectors and summarizes their usage.

Table 43. Backplane connectivity summary

Connector	Channel	Port	Board usage	PICMG definition	Comments
P10	48V	A/B	Power	3.0	Dual 48V DC power
	IPMB	A/B	IPMB	3.0	Dual IPMB
J23	Base 1	–	10/100/1000Base-T Port A	3.0	Dual star Base interface
	Base 2	–	10/100/1000Base-T Port B	3.0	
	Fabric 1	0	10G BASE-BX4/KX4 Port A lane 0 or 1000BASE-BX/KX Port A	3.1 Option 1 or 9	Dual star Ethernet Fabric interface
		1	10G BASE-BX4/KX4 Port A lane 1 or 1000BASE-BX/KX AMC Port 0	3.1 Option 2 or 9	
		2	10G BASE-BX4/KX4 Port A lane 2 or 1000BASE-BX/KX AMC Port 8	3.1 Option 9 or Undefined Option	
		3	10G BASE-BX4/KX4 Port A lane 3	3.1 Option 9 or unused	
	Fabric 2	0	10G BASE-BX4/KX4 Port B lane 0 or 1000BASE-BX/KX Port B	3.1 Option 9, Option 1 or Option 2	Dual star Ethernet Fabric interface
		1	10G BASE-BX4/KX4 Port B lane 1 or 1000BASE-BX/KX AMC Port 1	3.1 Option 9 or Option 2	
		2	10G BASE-BX4/KX4 Port B lane 2 or 1000BASE-BX/KX AMC Port 9	3.1 Option 9 or Undefined Option	
		3	10G BASE-BX4/KX4 Port B lane 3	3.1 Option 9 or unused	
J20	Update	0	AMC Site “Fastpath” update channel port 12	3.0	For AMC APS
	Update	4	AMC Site “Slowpath”	3.0	For AMC APS
	Clock	1A/1B	Input: 8 kHz	3.0	Multiplexed to AMC bay TCLKA, TCLKC
		2A/2B	Input: 19.44 MHz	3.0	
		3A/3B	Output	3.0	Multiplexed from AMC bay TCLKB, TCLKD

Zone 1 P10 connector pinout

Table 44 lists the P10 connector pinout.

Table 44. Zone 1 contact assignments, P10

Contact	Designation	Description	Mating sequence
1	Reserved	Reserved	*not applicable*
2	Reserved	Reserved	*not applicable*
3	Reserved	Reserved	*not applicable*
4	Reserved	Reserved	*not applicable*
5	HA0	Hardware Address Bit 0	Third
6	HA1	Hardware Address Bit 1	Third
7	HA2	Hardware Address Bit 2	Third
8	HA3	Hardware Address Bit 3	Third
9	HA4	Hardware Address Bit 4	Third
10	HA5	Hardware Address Bit 5	Third
11	HA6	Hardware Address Bit 6	Third
12	HA7/P	Hardware Address Bit 7 (Odd Parity Bit)	Third
13	SCL_A	IPMB Clock, Port A	Third
14	SDA_A	IPMB Data, Port A	Third
15	SCL_B	IPMB Clock, Port B	Third
16	SDA_B	IPMB Data, Port B	Third
17			
18			
19			
20			
21			
22			
23			
24			
25	SHELF_GND	Shelf Ground (Connection to Shelf Ground and safety ground)	First
26	LOGIC_GND	Logic Ground (Ground reference and return for front blade-to-front blade logic signals)	First
27	ENABLE_B	Enable B (Short pin for power sequencing, Feed B, tied to VRTN_B on Backplane)	Fourth
28	VRTN_A	Voltage Return A (–48 Volt return, Feed A)	First
29	VRTN_B	Voltage Return B (–48 Volt return, Feed B)	First
30	EARLY_A	–48 Volt Early A (–48 Volt input, Feed A precharge)	First
31	EARLY_B	–48 Volt Early B (–48 Volt input, Feed B precharge)	First
32	ENABLE_A	Enable A (Short pin for power sequencing, Feed A, tied to VRTN_A on Backplane)	Fourth
33	–48V_A	–48 Volt A (–48 Volt input, Feed A, uses ENABLE_A to enable converters)	Second
34	–48V_B	–48 Volt B (–48 Volt input, Feed B, uses ENABLE_B to enable converters)	Third
	Gray indicates unused pins		

Zone 2 J20 connector pinout

Table 45 lists the J20 connector pinout.

Table 45. Backplane connector J20 signals

Row	Interface designation	AB		CD		EF		GH	
1	Clks	CLK1A+	CLK1A–	CLK1B+	CLK1B–	CLK2A+	CLK2A–	CLK2B+	CLK2B–
2	Update Channel and Clks	Tx4(UP)+	Tx4(UP)–	Rx4(UP)+	Rx4(UP)–	CLK3A+	CLK3A–	CLK3B+	CLK3B–
3									
4		Tx0(UP)+	Tx0(UP)–	Rx0(UP)+	Rx0(UP)–				
5	Fabric Channel 15								
6									
7	Fabric Channel 14								
8									
9	Fabric Channel 13								
10									
Note: Each differential pair has an individual L-shaped ground contact (not shown).									
	Gray indicates unused pins								

Zone 2 J23 connector pinout

Table 46 lists the J23 connector pinout.

Table 46. Backplane connector J23 signals

Row	Interface designation	AB		CD		EF		GH	
1	Fabric Channel 2	Tx2[2]+	Tx2[2]–	Rx2[2]+	Rx2[2]–	Tx3[2]+	Tx3[2]–	Rx3[2]+	Rx3[2]–
2		Tx0[2]+	Tx0[2]–	Rx0[2]+	Rx0[2]–	Tx1[2]+	Tx1[2]–	Rx1[2]+	Rx1[2]–
3	Fabric Channel 1	Tx2[1]+	Tx2[1]–	Rx2[1]+	Rx2[1]–	Tx3[1]+	Tx3[1]–	Rx3[1]+	Rx3[1]–
4		Tx0[1]+	Tx0[1]–	Rx0[1]+	Rx0[1]–	Tx1[1]+	Tx1[1]–	Rx1[1]+	Rx1[1]–
5	Base Channel 1	BI_DA1+	BI_DA1–	BI_DB1+	BI_DB1–	BI_DC1+	BI_DC1–	BI_DD1+	BI_DD1–
6	Base Channel 2	BI_DA2+	BI_DA2–	BI_DB2+	BI_DB2–	BI_DC2+	BI_DC2–	BI_DD2+	BI_DD2–
7	Base Channel 3								
8	Base Channel 4								
9	Base Channel 5								
10	Base Channel 6								
Note: Each differential pair has an individual L-shaped ground contact (not shown).									
	Gray indicates unused pins								

RTM interface pinout

Zone 3 J30 connector pinout

Table 47 lists the Zone 3 J30 connector pinout.

Table 47. RTM connector J30 signals

Row	AB		CD		EF		GH	
1	+12V_RTM	+12V_RTM	+12V_RTM	+3.3V_IPMC		RTM_PRSNT*	RTM_HS_LED	RTM_EN*
2	+12V_RTM	+12V_RTM	+12V_RTM		IPMC_I2C_CLK	IPMC_I2C_DAT	USB_D+	USB_D–
3	SERIAL_0_TX	SERIAL_0_RX	JTAG_TDI	JTAG_TDO	JTAG_TMS	JTAG_TCK	JTAG_TRST	
4			INT_0	INT_1	RTML_TX	RTML_RX	RTML_CLK	RTM_RESET
5								
6							UC_SCL	UC_SDA
7								
8								
9	SAS0_TX+	SAS0_TX–	SAS0_RX+	SAS0_RX–	SAS1_TX+	SAS1_TX–	SAS1_RX+	SAS1_RX–
10	GE1_TX+	GE1_TX–	GE1_RX+	GE1_RX–	GE0_TX+	GE0_TX–	GE0_RX+	GE0_RX–
Note: Each differential pair has an individual L-shaped ground contact (not listed).								
	Gray indicates unused pins							

Zone 3 J31 connector pinout

Table 48 lists the Zone 3 J31 connector pinout.

Table 48. RTM connector J31 signals

Row	AB		CD		EF		GH	
1	PCIE_RX14+	PCIE_RX14-	PCIE_TX14+	PCIE_TX14-	PCIE_RX15+	PCIE_RX15-	PCIE_TX15+	PCIE_TX15-
2	PCIE_RX12+	PCIE_RX12-	PCIE_TX12+	PCIE_TX12-	PCIE_RX13+	PCIE_RX13-	PCIE_TX13+	PCIE_TX13-
3	PCIE_RX10+	PCIE_RX10-	PCIE_TX10+	PCIE_TX10-	PCIE_RX11+	PCIE_RX11-	PCIE_TX11+	PCIE_TX11-
4	PCIE_RX8+	PCIE_RX8-	PCIE_TX8+	PCIE_TX8-	PCIE_RX9+	PCIE_RX9-	PCIE_TX9+	PCIE_TX9-
5	PCIE_RX6+	PCIE_RX6-	PCIE_TX6+	PCIE_TX6-	PCIE_RX7+	PCIE_RX7-	PCIE_TX7+	PCIE_TX7-
6	PCIE_RX4+	PCIE_RX4-	PCIE_TX4+	PCIE_TX4-	PCIE_RX5+	PCIE_RX5-	PCIE_TX5+	PCIE_TX5-
7	PCIE_ REFCLK2+	PCIE_ REFCLK2-	PCIE_ REFCLK1+	PCIE_ REFCLK1-			PCIE_ REFCLK0+	PCIE_ REFCLK0-
8	PCIE_RX2+	PCIE_RX2-	PCIE_TX2+	PCIE_TX2-	PCIE_RX3+	PCIE_RX3–	PCIE_TX3+	PCIE_TX3-
9			SFP1_SCL	SFP1_SDA	SFP0_SCL	SFP0_SDA		
10	PCIE_RX0+	PCIE_RX0-	PCIE_TX0+	PCIE_TX0-	PCIE_RX1+	PCIE_RX1-	PCIE_TX1+	PCIE_TX1-
Note: Each differential pair has an individual L-shaped ground contact (not listed).								
	Gray indicates unused pins							

Onboard switches, headers, and connectors

Onboard switches

There are two switches on the CPM, both on the front panel, as follow:

- The reset switch
- The hot swap eject switch

The recessed reset push button (SW1) is located in the lower half of the front panel, just above the Base/Fabric channel Status LEDs (see Figure 2 on page 17).

The hot swap eject switch is connected to the lower blade latch assembly. When the latch is opened, it causes the switch to signal to the IPMC that a hot swap of the blade is desired. The IPMC monitors the process and controls the front panel H/S LED status. When the H/S LED turns steady blue, the top and bottom latches can then be used to eject the blade so it can be replaced. Refer to Table 2 on page 19 for details on the H/S LED status.

Onboard headers

There are several CPM onboard headers, but only the Customer header (P2) is available during normal operation. Refer to Figure 3 on page 18 for the location of the Customer header. In order to gain access to the Customer header, you will first need to remove the CPM from its slot (see *Removing the CPM* on page 71), and then remove the CPM cover (see *Removing the CPM board cover* on page 72). Table 49 lists the header pin pairs and the actions associated with an installed jumper.

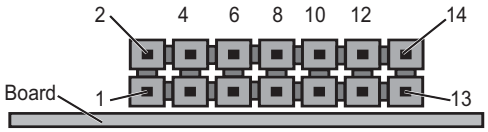


Table 49. Customer header (P2)

Pin Pair	No Jumper	Jumper Installed
1-2	N/C	Assert Clear NVRAM
3-4	Enable Boot Block Write	Boot Block Write Protect
5-6	N/C	BIOS Force Recovery
7-8	Enable eUSB Flash Write	eUSB Flash Write Protect
9-10	Enable UNR Shutdown	Disable UNR Shutdown
11-12	N/C	ME Firmware Recovery Mode
13-14	N/C	N/C

When installed, each jumper causes the following actions:

1-2 Assert Clear NVRAM The BIOS restores the NVRAM defaults on every boot when this jumper is installed.

3-4 Boot Block Write Protect Asserts the WP* signal to the flash to prevent any changes to the boot block region after the BIOS has set the appropriate lock bits.

5-6 BIOS Force Recovery The BIOS force recovery routine will execute on every boot when this jumper is installed.

7-8 eUSB Flash Write Protect The write protect input to installed eUSB devices is asserted when this jumper is in place.

9-10 Disable UNR Shutdown Prevents the IPMC from shutting down a blade when an upper non-recoverable (UNR) threshold is exceeded.

11-12 ME Firmware Recovery Mode Causes the ME firmware to stay in the recovery boot loader.

Onboard connectors

The CPM has a number of onboard connectors and other components that are used to expand onboard capabilities. The debug connectors along with the onboard power supply LED indicators are normally used only by development, manufacturing, and troubleshooting personnel. The remaining onboard connectors are useful to expand onboard memory and communications.The following onboard connectors are covered in more detail:

- MXM connector
- Dual micro SAS connector
- eUSB connector
- SATA connector

The following sections provide more detail on these connectors.

MXM connector

The onboard MXM connector is used by two types of Mobile PCI eXpress Module (MXM) devices; a supported Type A MXM 3.0 video module or the Radisys Dual Solid State Drive (DSSD) MXM module. Both types of supported modules derive all input, output, and power resources from the MXM connector. The pinout for the MXM connector is defined in the MXM 3.0 specification and is also listed in Table 50.

Table 50. MXM 3.0 connector pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
E1	+12V	E2	+12V	141	PE3_CPU0_RX_C_DN<1>	142	PE3_CPU0_TX_DN<1>
E3	GND	E4	GND	143	PE3_CPU0_RX_C_DP<1>	144	PE3_CPU0_TX_DP<1>
1	+5V_MXM	2	MXM_PRSNT_R*	145	GND	146	GND
3	+5V_MXM	4	NC	147	PE3_CPU0_RX_C_DN<0>	148	PE3_CPU0_TX_DN<0>
5	+5V_MXM	6	MXM_PWR_GOOD	149	PE3_CPU0_RX_C_DP<0>	150	PE3_CPU0_TX_DP<0>
7	+5V_MXM	8	MXM_PWR_EN	151	GND	152	GND
9	+5V_MXM	10	NC (Reserved)	153	CLK100M_MXM_PCIE_N	154	MXM_CLK_EN_R*
11	GND	12	NC (Reserved)	155	CLK100M_MXM_PCIE_P	156	MXM_PERST*
13	GND	14	NC (Reserved)	157	GND	158	NC
15	GND	16	NC (Reserved)	159	NC (Reserved)	160	NC
17	GND	18	MXM_PWR_LEVEL	161	NC (Reserved)	162	NC
19	MXM_STD_SW*	20	MXM_TH_OVERT*	163	NC (Reserved)	164	NC
21	NC	22	MXM_TH_ALERT*	165	NC (Reserved)	166	GND
23	NC	24	NC	167	NC (Reserved)	168	NC
25	NC	26	NC	169	NC	170	NC
27	NC	28	NC	171	NC	172	NC
29	HDMI_CEC	30	NC	173	GND	174	GND
31	NC	32	I2C3_PLOAD_SDA	175	NC	176	NC
33	NC	34	I2C3_PLOAD_SCL	177	NC	178	NC
35	NC	36	GND	179	GND	180	GND
37	GND	38	NC	181	NC	182	NC
39	NC	40	NC	183	NC	184	NC
41	NC	42	NC	185	GND	186	GND
43	NC	44	MXM_CUSTOM_ID0	187	NC	188	NC
45	MXM_CUSTOM_ID1	46	GND	189	NC	190	NC
47	GND	48	PE3_CPU0_TX_DN<15>	191	GND	192	GND
49	PE3_CPU0_RX_C_DN<15>	50	PE3_CPU0_TX_DP<15>	193	NC	194	NC
51	PE3_CPU0_RX_C_DP<15>	52	GND	195	NC	196	NC
53	GND	54	PE3_CPU0_TX_DN<14>	197	GND	198	GND
55	PE3_CPU0_RX_C_DN<14>	56	PE3_CPU0_TX_DP<14>	199	NC	200	NC
57	PE3_CPU0_RX_C_DP<14>	58	GND	201	NC	202	NC
59	GND	60	PE3_CPU0_TX_DN<13>	203	GND	204	GND
61	PE3_CPU0_RX_C_DN<13>	62	PE3_CPU0_TX_DP<13>	205	NC	206	NC
63	PE3_CPU0_RX_C_DP<13>	64	GND	207	NC	208	NC
65	GND	66	PE3_CPU0_TX_DN<12>	209	GND	210	GND
67	PE3_CPU0_RX_C_DN<12>	68	PE3_CPU0_TX_DP<12>	211	NC	212	NC
69	PE3_CPU0_RX_C_DP<12>	70	GND	213	NC	214	NC

Table 50. MXM 3.0 connector pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
71	GND	72	PE3_CPU0_TX_DN<11>	215	GND	216	GND
73	PE3_CPU0_RX_C_DN<11>	74	PE3_CPU0_TX_DP<11>	217	NC	218	NC
75	PE3_CPU0_RX_C_DP<11>	76	GND	219	NC	220	NC
77	GND	78	PE3_CPU0_TX_DN<10>	221	GND	222	GND
79	PE3_CPU0_RX_C_DN<10>	80	PE3_CPU0_TX_DP<10>	223	NC	224	NC
81	PE3_CPU0_RX_C_DP<10>	82	GND	225	NC	226	NC
83	GND	84	PE3_CPU0_TX_DN<9>	227	NC (Reserved)	228	GND
85	PE3_CPU0_RX_C_DN<9>	86	PE3_CPU0_TX_DP<9>	229	NC (Reserved)	230	NC
87	PE3_CPU0_RX_C_DP<9>	88	GND	231	NC (Reserved)	232	NC
89	GND	90	PE3_CPU0_TX_DN<8>	233	NC (Reserved)	234	NC
91	PE3_CPU0_RX_C_DN<8>	92	PE3_CPU0_TX_DP<8>	235	NC (Reserved)	236	NC
93	PE3_CPU0_RX_C_DP<8>	94	GND	237	NC (Reserved)	238	NC (Reserved)
95	GND	96	PE3_CPU0_TX_DN<7>	239	NC (Reserved)	240	NC (Reserved)
97	PE3_CPU0_RX_C_DN<7>	98	PE3_CPU0_TX_DP<7>	241	NC (Reserved)	242	NC (Reserved)
99	PE3_CPU0_RX_C_DP<7>	100	GND	243	NC (Reserved)	244	GND
101	GND	102	PE3_CPU0_TX_DN<6>	245	NC (Reserved)	246	NC
103	PE3_CPU0_RX_C_DN<6>	104	PE3_CPU0_TX_DP<6>	247	NC (Reserved)	248	NC
105	PE3_CPU0_RX_C_DP<6>	106	GND	249	NC (Reserved)	250	GND
107	GND	108	PE3_CPU0_TX_DN<5>	251	GND	252	NC
109	PE3_CPU0_RX_C_DN<5>	110	PE3_CPU0_TX_DP<5>	253	DP_A_L0_N_MXM	254	NC
111	PE3_CPU0_RX_C_DP<5>	112	GND	255	DP_A_L0_P_MXM	256	GND
113	GND	114	PE3_CPU0_TX_DN<4>	257	GND	258	NC
115	PE3_CPU0_RX_C_DN<4>	116	PE3_CPU0_TX_DP<4>	259	DP_A_L1_N_MXM	260	NC
117	PE3_CPU0_RX_C_DP<4>	118	GND	261	DP_A_L1_P_MXM	262	GND
119	GND	120	PE3_CPU0_TX_DN<3>	263	GND	264	NC
121	PE3_CPU0_RX_C_DN<3>	122	PE3_CPU0_TX_DP<3>	265	DP_A_L2_N_MXM	266	NC
123	PE3_CPU0_RX_C_DP<3>	124	GND	267	DP_A_L2_P_MXM	268	GND
125	GND	126	KEY	269	GND	270	NC
127	KEY	128	KEY	271	DP_A_L3_N_MXM	272	NC
129	KEY	130	KEY	273	DP_A_L3_P_MXM	274	NC
131	KEY	132	KEY	275	GND	276	DP_A_HPD
133	GND	134	GND	277	DP_A_AUX_N_DDC_CLK	278	+3_3V_MXM
135	PE3_CPU0_RX_C_DN<2>	136	PE3_CPU0_TX_DN<2>	279	DP_A_AUX_P_DDC_DAT	280	+3_3V_MXM
137	PE3_CPU0_RX_C_DP<2>	138	PE3_CPU0_TX_DP<2>	281	MXM_PRSNT_L*		
139	GND	140	GND				

Note: Signal names followed with * indicate that the signal is active low.
Pins listed as “NC (Reserved)” must be kept unconnected to allow for future use.

The DSSD MXM module uses available power and other signals on the MXM connector that do not interfere with any video modules that might also supported on the connector.

Dual micro SAS connector

A dual stacked micro-SAS connector is included on the SDDS MXM module to support the installation of two 1.8" micro SATA SSD drives. Table 51 lists the pinout for the dual micro SAS connectors.

Table 51. Dual micro SAS connector pinout

Lower Pins	Signal	Upper Pins	Signal
P1A	+3_3V	P1B	+3_3V
P2A	+3_3V	P2B	+3_3V
P3A	GND	P3B	GND
P4A	GND	P4B	GND
P5A	+5V (Stuffing option)	P5B	+5V (Stuffing option)
P6A	+5V (Stuffing option)	P6B	+5V (Stuffing option)
P7A	NC	P7B	NC
P8A	NC	P8B	NC
P9A	NC	P9B	NC
S1A	GND	S1B	GND
S2A	SATA_RX0+	S2B	SATA_RX1+
S3A	SATA_RX0-	S3B	SATA_RX1-
S4A	GND	S4B	GND
S5A	SATA_TX0-	S5B	SATA_TX1-
S6A	SATA_TX0+	S6B	SATA_TX1+
S7A	GND	S7B	GND
S8A	GND	S8B	GND
S9A	NC	S9B	NC
S10A	NC	S10B	NC
S11A	GND	S11B	GND
S12A	NC	S12B	NC
S13A	NC	S13B	NC
S14A	GND	S14B	GND
A1A	NC	A2A	NC
A2A	NC	A2B	NC

eUSB connector

There are two Embedded Universal Serial Bus (eUSB) connectors located between the J20 and J23 backplane connectors at the back edge of the CPM. These connectors can accept one or two dual stackable eUSB flash modules. Table 52 lists the pinout for each of the eUSB connectors.

Table 52. eUSB connector pinout

Pin	Signal	Pin	Signal
1	EUSB_RST*	6	GND
2	EUSB_WP*	7	USB+
3	NC	8	USB-
4	NC	9	GND
5	+3.3V		

SATA connector

The onboard SATA connector makes it possible to connect an external SATA device to the CPM and control it using the PCH SATA controller. The external SATA device will need to receive power externally as well. The onboard SATA connector is located near the upper front panel of the CPM between any installed MXM module and the front panel. Table 53 lists the pinout for the onboard SATA connector.

Table 53. SATA connector pinout

Pin	Signal	Pin	Signal
1	GND	5	SATA_RXN
2	SATA_TXP	6	SATA_RXP
3	SATA_TXN	7	GND
4	GND		